White Paper 3
System Level ESD
Part III: Review of IEC 61000-4-2 ESD Testing and Impact on System-Efficient ESD Design (SEED)

Industry Council on ESD Target Levels

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This document is available through various public domains as listed below:

The Industry Council on ESD
http://www.esdindustrycouncil.org/ic/en/

The Electrostatic Discharge Association
http://www.esda.org/

JEDEC – Under Publication JEP163
http://www.jedec.org/

Abstract

This document is the third of the Industry Council white papers dealing with System Level Electrostatic Discharge (ESD). The previous two white papers addressing system level ESD are the Industry Council's WP3 Part I and WP3 Part II.

In WP3 Part I, the misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified, and a novel ESD component / system co-design approach called system efficient ESD design (SEED) was described. The SEED approach is a comprehensive ESD design strategy for system interfaces to prevent hard (permanent) failures. In WP3 Part II this comprehensive analysis of system ESD understanding to categorize all known system ESD failure types was expanded, and described new detection techniques, models, and improvements in design for system robustness. WP 3 Part II also expands this SEED co-design approach to include additional hard / soft failure cases internal to the system.

This third document on system level ESD takes this further while focusing on system testing of ports and the shortcomings of air discharge testing.

Part A of the document highlights the need of a consistent and standardized specification of IO Port contact discharge which is widely used in industry. This is supported by real world discharge scenarios like cable discharge. A well specified testing procedure and the related target levels for IO port direct pin injection are the base for a SEED simulation and co-design approach which can commonly be executed by IC suppliers and system customers.

Part B addresses air discharge testing, which is most relevant for field fails, while its specification in IEC 61000-4-2 and its practical application suffers from both missing repeatability and reproducibility. In the first part, the arguments of maintaining air discharge as a relevant, mandatory test method are explained. Various scenarios leading to real world discharge events which correlate to IEC 61000-4-2 testing are analyzed in more detail. They can lead to soft and hard fails reproducible by system ESD testing. Secondly, in this document new considerations to better calibrate the air discharge test and reliably perform a repeatable air discharge test are given.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, OEMs, ESD tester manufacturers, ESD consultants and ESD IP companies.

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Mission Statement

The Industry Council on ESD Target Levels was founded on its original mission to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by downscaled process technologies on practical protection designs, the Council provides a consolidated recommendation for future ESD target levels. The Council Members and Associates promote these recommended targets for adoption as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies.

In response to the growing prevalence of system level ESD issues, the Council has now expanded its mission to directly address one of the most critical underlying problems: insufficient communication and coordination between system designers (OEMs) and their IC providers. A key goal is to demonstrate and widely communicate that future success in building ESD robust systems will depend on adopting a consolidated approach to system level ESD design. To ensure a broad range of perspectives the Council has expanded its roster of Members and Associates to include OEMs as well as experts in system level ESD design and test.

Preface

This white paper presents the recent knowledge of system ESD field events and air discharge testing methods. Testing experience with the IEC 61000-4-2 (2008) and the ISO 10605 ESD standards has shown a range of differing interpretations of the test method and its scope. This often results in misapplication of the test method and a high test result uncertainty. This white paper aims to explain the problems observed and to suggest improvements to the ESD test standard and to enable a correlation with a SEED IC/PCB co-design methodology. This white paper is divided into a part on direct pin stressing (Part A) and IEC 61000-4-2 testing of chassis and display which is typically a type of air discharge (Part B). Part A discusses the necessary industry alignments and standardization to support a unified SEED design procedure. Part B provides the input to improve the calibration and test reliability of IEC 61000-4-2 in the air discharge mode.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group associated with JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies, contract manufacturers and OEMs. The data represents information collected for the specific analysis presented here; no specific components or systems are identified.

The Industry Council, while providing this information, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

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Glossary of Terms

AC	alternating current
ADS	Advanced Design System
ASIC	application specific integrated circuit
CAN	controller area network
CAT	category
CDE	cable discharge event
CDM	charged device model
CST	Computer Simulation Technology
DAC	direct attach copper
DC	direct current
DNA	deoxyribonucleic acid
DUP	device under protection
DUT	device under test
DVI	digital visual interface
EOS	electrical overstress
ESD	electrostatic discharge
EUT	equipment under test
FDTD	finite-difference time-domain
FIT	finite integration technique
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
HBM	human body model
HCP	horizontal coupling plane
HDMI	high definition multimedia interface
H-M	human-metal
IBIS	input/output buffer information specification
IC	integrated circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IO	input/output
ISO	International Organization of Standards
IV	current-voltage
LAN	local area network
LCD	liquid crystal display
PC	personal computer
PCB	printed circuit board
PHY	physical layer interface
PIFA	planar inverted F antenna
PoE	power over Ethernet
RC	resistor capacitor network
RF	radio frequency
RH	relative humidity
RLC	resistor inductor capacitor network
SEED	system efficient ESD design
SFP	small form-factor pluggable
SPICE	simulation program with integrated circuit emphasis

TLM	transmission line matrix
TVS	transient voltage suppression
USB	universal serial bus
UTP	unshielded twisted pair
UV	ultraviolet
WB	wet bulb
VCP	vertical coupling plane

Definitions

EMC: electromagnetic compatibility – The condition which prevails when telecommunications (communication-electronic) equipment is collectively performing its individual designed functions in a common electromagnetic environment without causing or suffering unacceptable degradation due to electromagnetic interference to or from other equipment/systems in the same environment (MIL-STD-463A).

SEED: system-efficient ESD design - Co-design methodology of on-board and on-chip ESD protection to achieve system level ESD robustness.

Soft Failure: Failure of a system, not due to physical damage, in which the system can be returned to a functional state without the repair or replacement of a component. Return to a functional state may or may not require operator intervention. Operator intervention may include rebooting or power cycling. Soft Failures can involve software issues and software fixes but in the context of this document they are primarily due to ESD events injecting unwanted signals into the system which place the system into a state in which it does not function as intended.

Executive Summary

The Industry Council previously published two white paper documents describing the nature of component level electrostatic discharge (ESD) versus system level ESD, and the methods to ensure efficient system level ESD robustness. WP3 Part 1, also known as JEP 161, established that there is no correlation between component and system level robustness and introduced the concept of *system-efficient ESD design*, known as SEED, while WP3 Part 2 (JEP 162) expands on the concept of SEED, which utilizes simulations to achieve desired system ESD robustness with minimal impact on system performance.

We present here White Paper 3 Part 3 that addresses real-world system level ESD testing and suggests improvements to the existing International Electrotechnical Commission (IEC) 61000-4-2 standard widely used to test for ESD reliability of electronic systems. Before presenting a summary of this new white paper, highlights of the two previous white papers are reviewed to place the challenges of system level ESD in a full perspective.

Review of WP3 Part 1 document highlights:

- The misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified.
- A novel ESD component / system co-design approach called system efficient ESD design (SEED) was described.

Review of WP3 Part 2 document highlights:

- Comprehensive analysis of system ESD understanding to categorize all known system ESD failure types and describe new detection techniques, models, and improvements in design for system robustness.
- Discussed system ESD stress application methods and introduces new system diagnosis methods to detect weak ESD failure areas leading to hard or soft failures.
- Outlined present-day state-of-the-art electromagnetic compatibility (EMC)/electromagnetic interference (EMI) design prevention methods that have been developed to prevent system level ESD failure.

Introductory Note for WP3 Part 3:
While the two previous documents have set the stage for approaching system level ESD in a more realistic manner, the nature of testing for the well-established IEC 61000-4-2 test method has not adequately addressed all the challenges of testing from an increasing variety of modern electronic systems. This third document on system level ESD is intended to be a comprehensive review of more effective test procedures and recommends them for consideration as part of an overall improved IEC 61000-4-2 test method.

Overview of the Document:
As an important note, compilation of this document involved contributions from university and industry experts and includes a survey of the most salient findings from published academic research papers. The main goal is to derive the most important information and to leverage this to formulate recommendations to an overall improved system level ESD test method.

What is the real motivation here?
All electronic systems, from mobile phones to large computers, need to be tested for robustness from damage or upset from electrostatic discharge. System ESD testing is done using an ESD pulse generator, often called an ESD gun. The vast majority of system level ESD testing follows the test procedures and ESD pulse generator specifications defined in IEC 61000-4-2. Unfortunately, even when carefully following the procedures in IEC 61000-4-2, there is a high level of uncertainty in the test results, and successfully passing the test requirements is often not a complete prediction of ESD robustness in the field.

The uncertainty in system level ESD test results is often attributed to the large differences in the calibration current waveforms which can exist between ESD guns from different manufacturers, even when all the ESD guns meet the specifications in IEC 61000-4-2. But this is only a part of the problem.

The reason the Industry Council has addressed this topic is regarding the need for a more relevant and reproducible system ESD test procedure to better correlate integrated circuit (IC) and board co-design approaches as discussed in WP3 Part 1 and Part 2. The Industry Council provides recommendations based on technical data in this document which can be used for further discussion in standardization committees which are chartered with system level ESD test methods.

This White Paper explores the reasons for the high level of uncertainty in the test results, proposing test procedure modifications to improve repeatability, reproducibility, and predictability in field performance. Modeling methods are also discussed which can give insight into system level ESD testing and the design of ESD robust systems.

Organization of the Document:
The document is divided into two main parts: Part A describes direct pin discharge, and Part B considers discharge to chassis and display, also known as air discharge. Specifically, Part A presents real world scenarios such as cable discharge events (CDE) to introduce an extension to the IEC 61000-4-2 standard on direct port discharging. To further facilitate this, reference circuit models are described so that SEED, as introduced in White Paper 3 Part 1, can be used more effectively. Whereas Part B describes the shortcomings of the currently practiced air discharge method and recommends improvements for calibration and test measurements.

Synopsis of Part A:
For shielded connectors, the IEC 61000-4-2 standard does not specify direct pin stress, but this is important for system qualification involving uncertain results, variations in individual set ups, and repeatability of the results. This section promotes an industry wide alignment for the IEC 61000-4-2 standard to include direct pin discharge. For printed circuit board (PCB) designs to address this issue, standard models for SEED are described.

In Part A of this document, the approach is first to describe the real-world events (Chapter 1) that must be understood, then detailing the direct-injection method (Chapter 2) and concluding with information on the important target levels for these tests (Chapter 3). For these issues on direct pin testing to be viewed in an analytical perspective, the ESD gun model details (Chapter 4) and the techniques of SEED simulations (Chapter 5) are also presented. An alternate characterization method using 50-ns TLP is also introduced that can be directly applied to the IC as a way of characterizing the external pin high current I-V response. One very important outcome of the

investigations is that for universal serial bus (USB) cables meeting standard shielding requirements a 2 kilovolts stress is enough.

Synopsis of Part B
After studying the air discharge test method, it is concluded that both a lack of precise test methods and specifications led to extreme variability and uncertainty in qualification results. Removing this method altogether is not an option since in the real-world events discharges to chassis do occur. Details of this inadequacy and the subsequent improved recommendations are given.

In Part B, the document focuses on improved test methods for displays using the air discharge method. This includes a review of the challenges associated with the IEC 61000-4-2 test methods and the test results' uncertainties (Chapter 6). Improvements to the calibration of the ESD simulators for both contact-mode discharge and air discharge are suggested (Chapter 7). With the extensive background of the test methods and the description of corresponding various opportunities for improved applications of these methods, the document recommendations useful test improvements (Chapter 8). Supporting technical details of the work presented in this document are given in the appendices at the end.

Nuances of System Level ESD Testing:
The most important points of this document can be understood only after the real issues of system level ESD robustness are clearly stated and defined. This will also give a better understanding of why the test method improvements recommended here are important to the industry.

System level ESD testing is performed using a combination of stresses to each system while in a powered, functional state. Contact discharge is applied to conductive surfaces by placing a pointed tip of the ESD gun against the system and initiating an ESD pulse. Air discharge is performed on insulative surfaces, with emphasis on locations frequently touched by the user, such as keyboards and touch screen displays, and locations where ESD can enter the system, such as seams, vent holes, etc. In this test a rounded tip on the ESD gun is charged to a high voltage and the gun is moved toward the system under test until an air discharge occurs or the surface of the system is touched. In the next test discharges are made to horizontal and vertical coupling planes near the device under test to see if the fields generated by these stresses can upset the system.

It is important to note that test results from system level ESD testing can have a variety of results:

- System suffers no ill effects from the testing
- Soft failure
    - System is upset but returns to normal operation without user intervention
    - System is upset but returns to normal operation after user intervention which may require a reboot of the system
- Hard failure in which there is permanent physical damage requiring repair.

The causes of testing uncertainty and failure to predict field reliability covered in this white paper are numerous and will be summarized here in bullet form.

- Important for both contact and air discharge

    - IEC 61000-4-2 compliant ESD guns have substantial variability in current waveforms and power distribution in the RF spectrum between models and manufacturers.
    - Number of stresses per discharge point (10) is insufficient to adequately predict soft failures, which can depend on precise timing between the stress and system timing.
    - Test results can depend on a previous stress if charge is not removed before the next stress - this phenomenon can lead to ***secondary discharge***.
    - Transient electromagnetic fields from ESD guns are not specified or limited. This leads to an uncertainty of soft failure testing with different guns. Pulse to pulse variation of the same gun can be eliminated by multi-zap testing.
- Contact discharge
    - Contact discharge is generally more repeatable than air discharge but does not represent the real world which is typically air discharge
    - Discharge current waveform is only verified for a low resistance load:
- Air discharge
    - There is no calibration procedure for ESD guns in air discharge
    - Test severity depends on arc length which is sensitive to a number of factors
        - Humidity
        - Approach speed
        - Geometry
        - Materials on each side of arc
- Discharge to coupling planes
    - Geometries specified in IEC 61000-4-2 are sometimes unrealistic for modern form factors
- Expanding the scope of IEC 61000-4-2
    - Cable discharge event (CDE) is not included
        - There are a number of forms of cable discharge event (CDE)
        - Cable quality can affect CDE
    - Tests conditions are not realistic for wearable devices, which could not have been realistically anticipated in the earlier IEC 61000-4-2 specification creation. These include items such as smart watches or mobile phones held in a case attached to a belt.

Important Recommendations from This Work:
Some important recommendations are summarized here for both contact discharge and air discharge tests.

Direct Discharge:

- Establish industry wide alignment for direct discharge to ports
- Consider alternate 50-ns TLP test with 2 ampere goal applied to IC pins
- Consider 2 kilovolts contact discharge as a standard spec for USB pins meeting cable shielding requirements

Air Discharge:

Consider recommendations to improve the testing at a chosen discharge point that include:

- Maintain air discharge as a field relevant stress method, but improve its reproducibility by:
    - Improved gun calibration for air discharges
    - Controlled arc length using
        - A well-controlled humidity environment
        - Introduction of ionization
    - Controlled approach conditions by use of robotics
    - Increased number of discharges per test point
    - Controlling secondary discharge
    - Measurement of radiated gun emission
- Address cable discharge as a relevant system level ESD event

Test Reproducibility Recommendations:

The white paper presents data to support an understanding of state-of-the-art system ESD testing and makes suggestions for improving the repeatability and reproducibility of system level ESD testing. The following bullet list summarizes the improved understanding and suggestions for improving future testing.

- ESD gun calibration
    - Contact discharge waveform verification with loads other than a low impedance resistive load
    - Introduction of a method for ESD gun calibration in air discharge mode without the uncertainties of air discharge
    - Measurement of radiated emissions, including the RF power spectrum
- Methods to improve air discharge arc repeatability
    - Ionization to stabilize arc length
    - Different air discharge tip materials
    - Improvements in temperature and humidity control
    - Charge removal techniques
    - Robotic testing to improve control of approach speeds
- Improvements in test procedures
    - Recommendations on increasing the number of stresses at each test location to improve capture of weaknesses due to soft failures
    - Improved understanding of ESD discharge voltage as a function of humidity
    - Robotics to improve test repeatability
    - Improvements in documentation of test procedures used, including video recording

Finally, the white paper also presents modeling methods which can both improve the understanding of system level ESD testing and help in the design of ESD robust systems.

- Simulation program with integrated circuit emphasis (SPICE) level models of ESD guns
- System Efficient ESD Design (SEED) for simulating systems when ESD stressed
- 3D models of ESD guns and systems

Part A: Direct Pin Discharge

Chapter 1: Real World Stress to Port Pins

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1.0 Introduction

The IEC 61000-4-2 test uses the discharge of a human via a handheld metal object as its reference ESD event. However, a variety of other ESD events occur which are not within the scope of the test standard. Many attempts have been made to use the IEC 61000-4-2 test generator to perform testing which will ensure robustness against other ESD events.

1.1 Human-Metal Discharge

The IEC 61000-4-2 standard uses the discharge of a human via a small metal part as its reference event [Chu2004]. The waveform shown in the IEC 61000-4-2 standard is similar to the discharge waveform of a human via a small handheld metal part at about 5 kilovolts at an arc length of 0.8 mm. Due to the nonlinear behavior of the arc, human-metal ESD discharges at shorter arc length will have faster rise times and longer arc lengths will have slower rise times. The reference event covers only one situation. Its current derivative is in the range of 4 A/ns, which is at the lower end of the current derivatives observed for human-metal ESD, over a large range of voltages and arc lengths.

1.2 Human Skin ESD

A human skin ESD has much longer rise times (in the range of 1-10 ns for < 8 kilovolts) and lower peak current values compared to a human-metal discharge. However, in the case of multiple discharge pulses, the subsequent pulses will have much faster rise times even if the amplitudes are lower.

1.3 Cables and Cable Discharge Events

In system level testing, discharges to connector pins should be included if the connector geometry allows for such discharges. This requires understanding of the threat levels. Directly applying IEC 61000-4-2 testing at system level voltage settings (e.g., 8 kilovolts) can lead to over testing and unnecessary additional costs. The situations which lead to connector currents need to be identified and the stress levels, as seen by the sensitive data wires, need to be determined and used as guidance for setting test levels.

If a charged cable is inserted into a device under test (DUT), a current will flow onto the connector. Typically, events which cause connector currents are:

- Discharge to a DUT which is connected to ground in a system from a charged source such as a USB cable
- Discharge to another DUT, when both DUTs are connected to each other by a cable.
- Attaching a charged DUT to a grounded cable or a docking station.

The present system level IEC 61000-4-2 standard does not consider a cable discharge event, often referred to in industry as cable discharge event (CDE). However, the IEC 61000-4-2 standard does give some guidance as to which part of a connector should be exposed to a direct ESD discharge.

Protection design and an appropriate testing of system input/outputs (IOs) is certainly a critical topic. Multiple companies have reported field failures on ports such as USB or local area network (LAN). The assumption that a discharge will be safe because the cable is properly shielded, and a ground contact will be made first due to connector design, is often not true. The analysis of cables bought from a wide range of cable suppliers has shown that about 30% of the USB2 cables did not have any shield connection. Missing shield connections have also been found on USB 3.1 cables [Mar2017c, Stad2017].

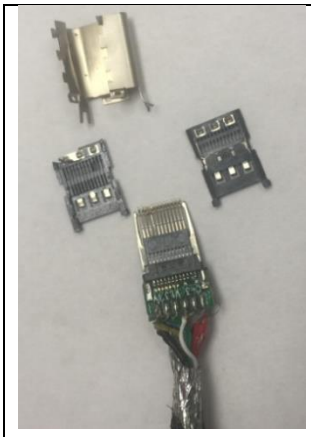
Due to faster IO speeds, and influenced by reduced human body model (HBM) and charged device model (CDM) robustness levels, more emphasis must be placed on the trade-off between PCB and IC level protection. This is covered by the SEED concept. To enable a SEED based design there must be an understanding of the amplitude and the waveform of the cable discharge. Real world conditions for cable discharges of LAN and USB cables are discussed in the following.

For Ethernet, one needs to distinguish between Ethernet ports that use a transformer, often referred to simply as "magnetics" at the port, and those which have a direct connection to the circuit. The transformer provides a high voltage isolation barrier of at least 1500 volts, and for short term, nanosecond long pulses probably > 5000 volts. It also provides a common mode return path via the Bob Smith termination circuit, and via ferrites for power over Ethernet (PoE) devices. Further, the transformer will saturate at rather low currents. This saturation will reduce the coupling between the primary and secondary side; thus, it reduces the coupling of the physical layer interface (PHY) IC. This section analyzes LAN interfaces, such as unshielded twisted pair (UTP), which uses a transformer.

In contrast, small form-factor pluggable (SFP) + direct attach copper (DAC) cables directly provide an entry path, without magnetics to the physical layer interface IC. These cables are shielded, have a shielded connector that mates at the shield first. However, direct discharges to the pins are, although not likely, possible. The ESD performance of such cables has not been investigated yet.

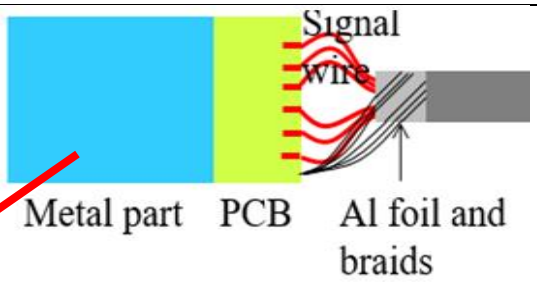
Cables have been found which allow discharges to the signal wires of a USB, as they contain ungrounded decorative metal parts above the unshielded signal wires and connector pins. The cable shown in Figure 1 had a decorative metal that is not connected to the shield or the connector. The decorative metal is above the signal wires which connect to a PCB which is within the connector. The signal wires are not shielded underneath the metal part, as the foil and braid are only connected

to an unshielded PCB on one side. This allows sparking between the unconnected, decorative metal and the signal wires of the cable and the PCB.



Front side

Back side and decorative metal after removal (lower photo)



Sketch showing the shield connection

Figure 1: Photo and drawing explaining the shield structure of a badly shielded USB 3.1 cable.

In general, CDE discharges are a rather complex process. The effect of CDE depends on:

- The charge voltage of the cable
- The charge mode (most cables will charge in common mode: All wires and the shield are at the same potential). A cable may also be polarized by a charge on the jacket. This charge will cause polarization of the metal structure, but no net charge on the metal structure. No matter whether the cable carries a net charge or if it is polarized, sparking can occur if the cable is inserted into a grounded connector.
- The type of shield structure: No shield, such as UTP; shield present but not connected; foil shield; foil + braid shield; connection of the shield to the connector from pigtail to 360° shield.
- The contact sequencing will vary from an undefined sequence, as every pin has the same chance to mate first, to a typical sequence observed in a good USB cable: Shell first, then GND or 5V, then data.
- Exposure of pins: Some connectors will not allow an ESD to a pin as the ESD will be diverted to the shell. However, other cables may not have a shell, or may not connect the shell and may allow direct ESD to pins.
- Probability of ESD: Connections like USB are inserted rather often, other connections, such as a video interface will be inserted into most devices less often.
- Form factor and chassis material: For example, some USB memory sticks often have no shield, no shell and may allow discharges via the plastic into the circuit.

To highlight the essential aspects, a brief analysis is provided for two interfaces; LAN and UTP. The details can be found in the cited literature and in Section 1.4 (for LAN).

1.3.1 Charging and Discharging of USB Cables

Electronic systems must tolerate electrostatic discharges in a typical user environment. The existence of badly shielded cables and poor contact between the shield and the connector requires studying real world waveforms for USB cable discharge events [Mar2017c, Stad2017]. Charged cable events have been investigated by charging a cable to a known voltage and then inserting the cable into a connector to measure the currents. However, environmental conditions and materials can change the charge level and related electrostatic charge voltage. But, for many practical cases, the voltages that a cable can reach via triboelectric charging are not well known. To address this concern, a set of experiments were conducted where the total accumulated charge was measured.

High charging voltages have been observed for:

- People sitting up from a chair
- People removing a garment, such as a fleece jacket
- Handling of plastic sheet material

The voltages reached by walking on a carpet are usually much lower than the voltages reached by the situations described above.

An experiment was conducted measuring the voltages on cables that were rubbed against various clothing materials. The aim of this study by Rezaei et al. was to enhance the understanding of cable charging behavior under different humidity conditions, with a variety of rubbing materials [Rez2017]. The voltage levels and various dependencies for such cable charging were investigated. The charge levels translate into a voltage if the capacitance of the cable to ground is considered. The insertion of a charged cable into a USB connector may lead to a CDE. Throughout this section the act of plugging in a cable is called a “plug-in event”. The USB cable connected devices are potential sources of a CDE. A CDE occurs because of the USB cable being charged and then discharging to the USB connector of the connected device. Typical examples include discharge scenarios such as an ESD to USB drive with no shield, a USB cable connected to cellphone inserted into a grounded device such as a personal computer (PC), a USB HUB connecting multiple electronic devices together via USB cables, etc. The goal of the work by Mardiguian et al. and Stadler et al. was to understand the range of stress levels seen by the USB 2.0 A/B (type A and type B connectors) cable connected devices due to various USB cable discharges as a function of the charging scenario, cable shield quality, and cable connections [Mar2017c, Stad2017].

1.3.2 Overview of Charging Scenario

Investigation on the effect of relative humidity and materials on triboelectric charging of USB cables was performed experimentally. The measurement setup involved the use of different sweater materials to rub on the outer jacket of various cables. This action of rubbing of different sweaters on cables led to the charging of cables by a triboelectric charging process. Figure 2 depicts one of the sweaters and one of the cables used in the study.

Figure 2: Rubbing of the sweater on the cable leads to a charge developed on the cable.

1.3.3 Overview of Discharge Scenarios

Various USB discharge scenarios are possible. For example, the direct ESD discharge to a USB drive, or a charged human holding a cable and plugging it into a USB connector. The focuses of the study were the discharge into a USB connected device and a discharge into a USB connector during a plug-in event. They are illustrated in Figures 3 and 4, respectively.

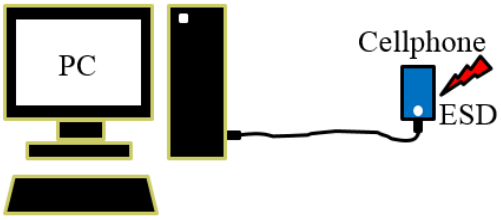


Figure 3: Discharge into a USB connected device scenario.

In Figure 3 a cellphone is connected to a grounded device such as a personal computer (PC) by a USB 2.0 cable. A charged human can discharge into the cellphone and the ESD discharge source point is at the cellphone. The current flows via the USB cable to the grounded PC. In Figure 4, a charged cable is inserted into the PC. The other end of the cable is connected to a USB device (a cell phone is depicted) which leads to a plug-in event.

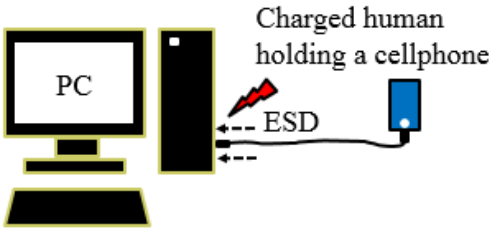


Figure 4: Discharge into a USB connector during a plug-in event.

1.3.4 Classification of USB 2.0 Cables Based on Shield Quality

In this study, randomly purchased USB 2.0 A/B cables (USB 2.0 type B to type A) are classified into three different types based on their cable shield quality. A resistor inductor capacitor network (RLC) meter was used to measure the USB connector shell to shell DC resistance of the cable. This gives a first impression on the shield's properties. If the resistance is within several hundred milliohm and does not change much when the cable is twisted, the cable is classified as a well-shielded cable. If the resistance is in the range of 1-80 ohms and it changes during twisting, the cable is classified as a badly shielded cable. A few of the USB 2.0 cables purchased had no shields. In addition, the shields of a few USB cables were cut for experimental purpose. Cables with a cut shield or no shield are classified as an unshielded cable.

1.3.5 Discharge into a USB Connected Device

A block diagram for this series of tests is shown in Figure 5. A 2 kilovolts contact mode ESD was injected into the conductive enclosure of the DUT box, resembling a situation in which an ESD occurs to a USB connected device (such as a USB drive) connected to a PC. For such a situation, data traffic can be active, while there cannot be data traffic during a plug-in event.

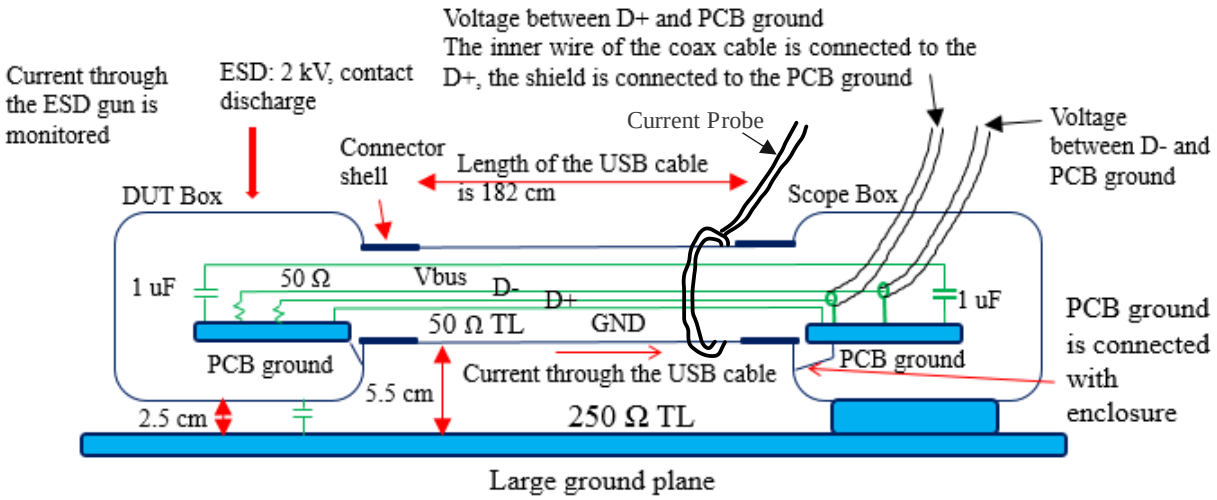


Figure 5: Discharge into a USB connected device.
Note: D+/D- lines terminated into 50-ohm impedance scope

The following figures show the common-mode current on the USB cable as captured by the F-65 monitoring probe clamped close to the scope box and the voltage induced between D+ and ground on the scope box side. The measured waveforms for the well-shielded, badly shielded, and unshielded USB cable types are shown in Figure 6.

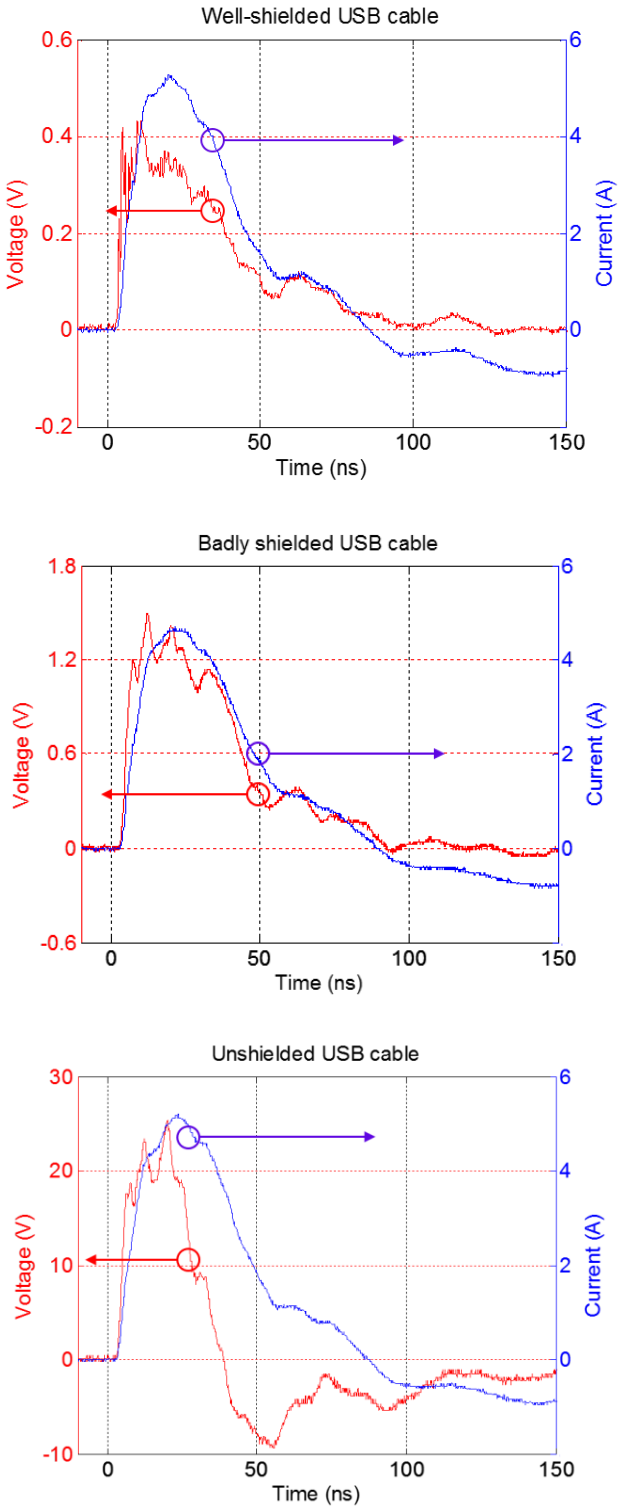


Figure 6: Common-mode current and voltage induced between D+ and ground for a discharge into a USB connected device scenario. Data is shown for well-shielded, badly shielded, and unshielded type USB cables. The ESD gun is discharged at 2 kV in contact mode. Note: the negative current readings are a measurement artifact of the F-65 current probe.

At a 2 kilovolts contact mode discharge, a noise voltage of 0.4 volts is measured for the well-shielded cable, 1.2 volts is measured for the badly shielded cable, and approximately 20 volts are measured for the unshielded cable (without taking the reaction of ESD protection into account). In contact mode the ESD gun discharge current has a linear relationship to the ESD gun voltage setting. If the same measurement is performed at a higher ESD gun voltage, the amplitude of the measured waveform is expected to increase linearly. At 2 kilovolts for an unshielded cable the peak current occurs at 20 ns and the amplitude is approximately 5 amperes as shown in Figure 6. The initial peak current would be 2 x 3.75 amperes, but it returns via the DUT box to ground capacitance and is therefore not visible in the F-65 current clamp data. The designer is often interested in a realistic worst-case specification. Although possible in some rare situations, direct discharges into pins were disregarded and the discharge into a USB connected device for the case of an unshielded USB cable was considered the realistic worst case.

If the ESD gun had been set at 8 kilovolts, a current amplitude of 20 amperes would be expected. It should be noted that the current measured using the F-65 current clamp is the common-mode current and it is not a function of the type of USB cable used. In the case of a badly shielded or unshielded cable it is reasonable that the common-mode current splits equally over the four wires of the USB 2.0 cable. Approximately a 5-amperes current will flow on each of the four wires, GND, Vbus, D+, and D-. This assumption is based on the fact that all wires are connected via low impedances to ground. The 5 volts (Vbus) is usually connected via a large value capacitor, and D+ and D- have ESD protection diodes either on the board or in the IC. A current of 5 amperes with pulse widths of 10's of nanoseconds on the IO lines (D+ and D-) can cause hard failures. Here the pulse width is not determined by the cable length, but by the source.

1.3.6 Discharge into a USB Connector during a Plug-in Event

When a charged person holds a cellphone connected to a USB cable, the charge will be distributed on the USB cable via polarization and/or charge migration. When the person inserts the USB cable into a grounded PC, ESD occurs. Figure 7 illustrates the test set-up used to investigate plug-in events.

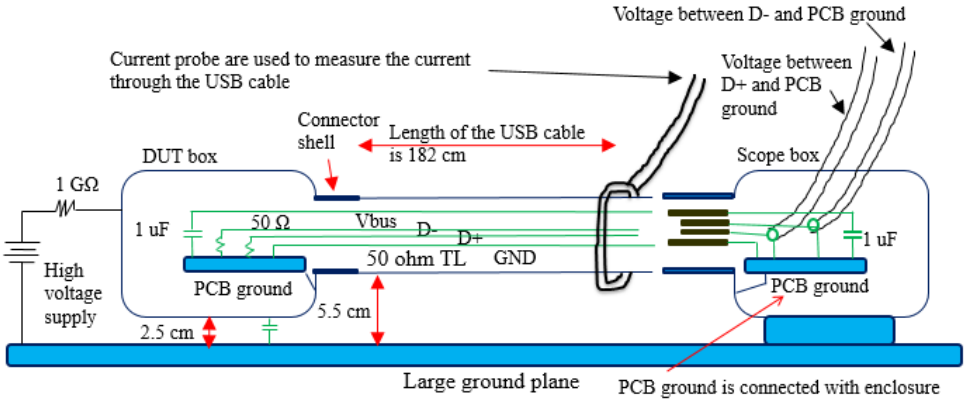


Figure 7: Discharge into a USB connector during a plug-in event.

Because of the design of the USB connectors, the shell will contact first, then the GND/Vbus pin follows, and finally D+/D- will contact. Even if the cable is unshielded, GND/Vbus will contact first.

1.3.6.1 Plug-in event sequencing

During the plug-in measurements the cable was charged via 1 GΩ. The unconnected end of the USB cable was held by hand using insulated gloves, then the operator inserted the cable into the scope box. Multiple pulses can occur during the insertion process. To be able to capture pulses that occur with microsecond delay times, a fast re-trigger mode was selected. Another application of the fast retrigger mode or sequence mode acquisition is shown in [Mar2017b], and [Mar2018], which explains the use of the fast re-trigger mode in capturing multiple pulses. The measurement was performed using ultra-segmentation (Rohde & Schwarz) or sequence mode acquisition (Teledyne LeCroy) activated on the oscilloscope. The oscilloscope can be triggered on the channel connected to the F-65 current clamp or the D+ signal.

The USB cable connector may not always enter the scope box in parallel to the connector. It may hit the scope box at an angle to be aligned for entering the scope box connector. This action leads to multiple triggers for a single plug-in event measurement. A possible sequence is illustrated in Figure 8.

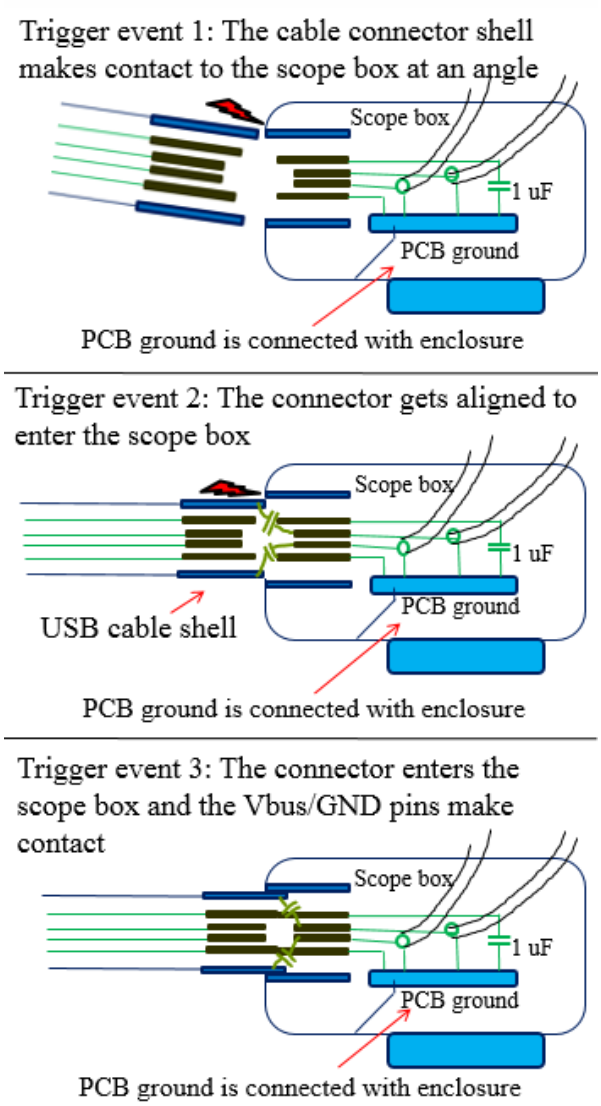


Figure 8: Plug-in event sequence is explained using three triggered events. It should be noted that multiple triggered events can occur in a plug-in measurement.

1.3.6.2 Plug-in event measurement results

A set of measured typical waveforms during a plug-in event is shown in Figure 9. They are based on charging the DUT box to 8 kilovolts and using a well-shielded cable. In this set-up the USB cable behaves as a transmission line (wire above the ground plane) having an impedance approximately equal to 266 Ω (1 kilovolt/3.75 amperes). In this measurement set-up, the USB cable GND wire was directly connected to the scope box PCB ground. The USB cable Vbus wire was terminated with a 1 uF capacitor on the PCB inside the scope box. Neither of these wires were monitored during the plug-in event measurements. However, emphasis was placed on the IO lines (D+ and D-) of the USB 2.0 cable. The waveforms induced on the D+ and the D- IO signal lines due to the plug-in event were comparable.

The F-65 current clamp, D+, and D- channels can be used to trigger the oscilloscope. In this case the oscilloscope was triggered on the D+ channel and the ultra-segmentation/sequence mode was enabled. It should be noted that the oscilloscope is triggered on the D+ channel to observe the waveforms induced on the IO signal lines due to the plug-in event. This leads to a few of the initial current waveforms through the USB cable not being acquired by the oscilloscope.

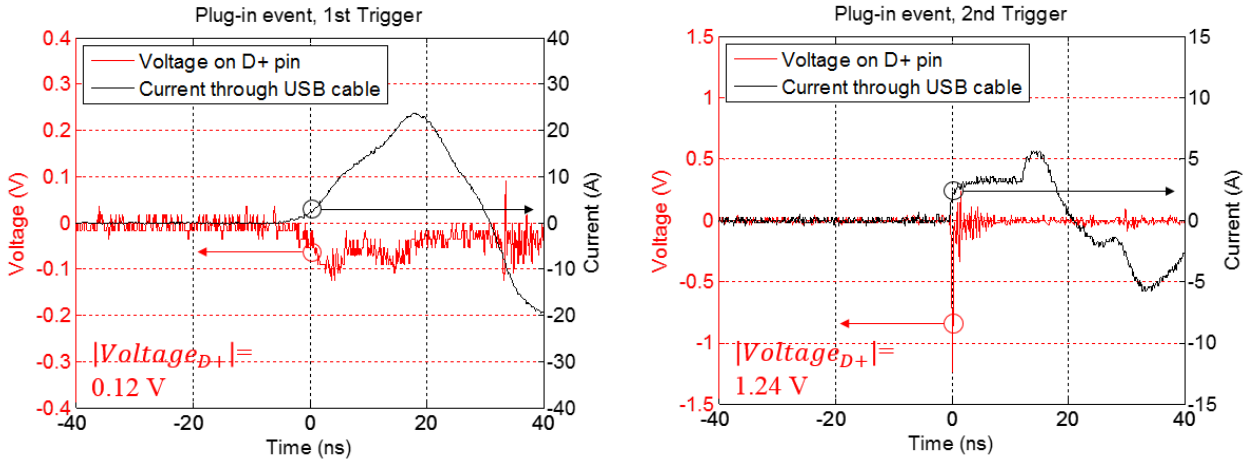


Figure 9: Discharge into a USB connector during a plug-in event. Measured waveforms for the first and second triggered event are shown.

During the plug-in sequencing, the first event caused lower ESD-induced voltage (0.12 V) on the D+ pin because most of the current flowed between the USB shell and the scope box. The second plug-in triggered event had a higher ESD-induced voltage on the D+ pin (1.24 volts).

1.3.7 Summary of USB Risks

A triboelectric charging scenario was investigated for various types of cables [Rez2017]. Two USB 2.0 cable discharge scenarios were investigated [Mar2017c, Stad2017]. The first scenario investigated ESD on a USB cable connected system. The second scenario investigated a plug-in event of a connected USB cable.

In the measured waveforms for the first discharge scenario, the discharge into a USB connected device shows pulse widths on D+ (IO signal) of 20-40 ns and 2-10 ns rise times at 2 kilovolts contact mode ESD to the USB connected device. If 8 kilovolts is set as the expected reliability level for the user environment, then the ESD protection needs to be able to handle 5 amperes for tens of

nanoseconds on the D+ and D- at the same time. Here, damage, as well as latch-up or soft failures may need to be considered. The plug-in of an already device-connected cable has a lower chance of causing damage. The voltages induced in D+ by a discharge between a USB cable and a grounded connector during the insertion show less than 5 volts at 8 kilovolts for the well-shielded and the badly shielded cables. For the case in which the USB cable has no shield, a voltage of approximately 12 volts has been induced at 8 kilovolts. This translates to a current of 0.24 amperes (oscilloscope channel impedance of 50 ohms) on the D+ IO line. It should be noted that even though this voltage amplitude may look significant, the duration of the pulse width is less than 10 ns as shown in Figure 9. Soft failures may still be possible if a cable is inserted into a USB HUB servicing multiple USB connections. Here, other active connections could be interrupted by the insertion of a charged USB cable even if the voltage is rather small.

The system designer must account for the fact that a large portion of the USB 2.0 cables on the market have no shield. About 1/3 of the thirty USB 2.0 cables randomly selected for this study had no shield or no shield to USB connector shell connection. ESD protection circuits should be designed to protect electronic device from CDE stress levels up to as much as 5 amperes for tens of nanoseconds on the D+/D- IO lines for an 8 kilovolts device stress level.

1.4 Cable Discharge of LAN Cables

1.4.1 Introduction

One needs to distinguish between Ethernet ports that use a transformer, often called magnetics at the port, and those which have a direct connection to the circuit. The transformer provides a high voltage isolation barrier of at least 1500 volts, and in the short term, nanosecond long pulses probably > 5000 volts. It also provides a common mode return path via the Bob Smith circuit, and via ferrites for PoE devices. Further, the transformer will saturate at rather low currents. This saturation will reduce the coupling between the primary and secondary side, thus, reducing the coupling of the physical layer interface IC. This section analyzes LAN interfaces, such as UTP, which use a transformer.

In contrast SFP + DAC cables (small form-factor pluggable + direct attach copper) directly provide an entry path, without magnetics, to the physical layer interface IC. These cables are shielded, having a shielded connector that mates at the shield first. However, direct discharges to the pins are, although not likely, possible. The ESD performance of such cables has not been investigated yet.

The protection strategies for an electronic system against ESD are mainly developed based on the type of ESD source, the discharge mechanism, and the likelihood of its occurrence. An IC located internal to an electronics system is at a lesser risk to an ESD event when compared to an IC having an interface that is exposed to the external world. For example, Ethernet physical layer (PHY) transceivers may be subjected to CDE, which is not the case for on board interfaces between ICs such as DDR interfaces.

When a charged LAN cable is plugged into an Ethernet connector [Gan2016], a cable discharge event will occur. The discharge voltage and subsequent current can damage the transformer, the common mode chokes, and especially the Ethernet PHY IC transceivers.

Over the past few years, researchers have understood that CDE needs to be treated separately from other types of ESD tests due to vast differences between the effects caused by CDE. LAN cable discharge pulses can be quite long and have the potential to stress the IO more than those discharges described by an HBM or IEC 61000-4-2 discharge model. Additionally, the LAN cable discharges lead to shorter rise times compared to the 0.8 ns rise time of the IEC 61000-4-2 standard. These shorter rise times may require faster turn on performance of the electrostatic discharge protection circuit. Some of the important differences are listed in the Table 1.

Table 1: Comparison between Different ESD Models

Parameter	HBM	CDM	IEC 61000-4-2	CDE
Rise time	2 to 10 ns	100 to 500 ps	~ 0.8 ns	100 to 300 ps
Pulse duration	150 ns,	~ 2 ns	~ 80 ns	up to several milliseconds (depends on the cable length)
Peak current	0.7A/kV	1- 16A (depends on the size of IC)	3.75 A/kV	Peak: ~5A/kV Plateau: ~3A/kV

The effects of LAN cable discharges leading to malfunction or even damage is presently not covered by any of the ESD immunity test methods. IEC 61000-4-2 is used to verify the ESD withstand capabilities, i.e. immunity of equipment, directly at its enclosure port and the metal shells of connector ports (excluding direct discharges to the pins). Complying with the system level IEC 61000-4-2 standard may not ensure enough robustness of the Ethernet system against LAN cable discharge. Several semiconductor manufacturers dealing with these communication interfaces have developed their own in-house CDE testers to qualify their ICs. However, the need for standardizing the test procedure is ever growing.

1.4.2 LAN Cable Charging Scenario

When a LAN cable is pulled over a surface, the cable may get charged due to a triboelectric effect. A LAN CDE can also occur if a person, who carries a laptop and is charged, inserts a LAN cable which is at ground potential. Other LAN CDE sources may be a charged device close to a cable which polarizes the cable.

The voltages of a LAN cable can appear between: (1) All twisted pairs and ground (common mode); (2) Wires of a single pair (differential mode); (3) Different pairs in the cable (mixed mode). The LAN cables can be charged in common mode and, although with a smaller likelihood, in differential mode. However, during the discharge sequence (pin sequencing) a cable which is charged in common mode can become charged in differential mode.

In [Gre2009], the average surface charge density on a short cable was experimentally measured by pulling it through an inline tribo-electrification charger consisting of a sleeve fabricated from numerous different plastic materials, including PTFE and aluminum, to provide friction against the cable jacket. The surface charge was measured using an electrometer. Examples of the surface charge measured densities are:

(1) For a PTFE charging sleeve: $\sigma = 0.1 * 10^{-8}$ C.cm^{-2};
(2) For aluminum charging sleeve: $\sigma = -0.15 * 10^{-8}$ C.cm^{-2}.

In another study [Wan2013a], a similar experiment has been performed where a spooled category (CAT) 6 cable is unwound over flooring materials like a high-pressure laminate, a typical surface material for a raised floor system. An example of the measured voltage (1.1 kilovolts) is shown in Figure 10 and Figure 11.

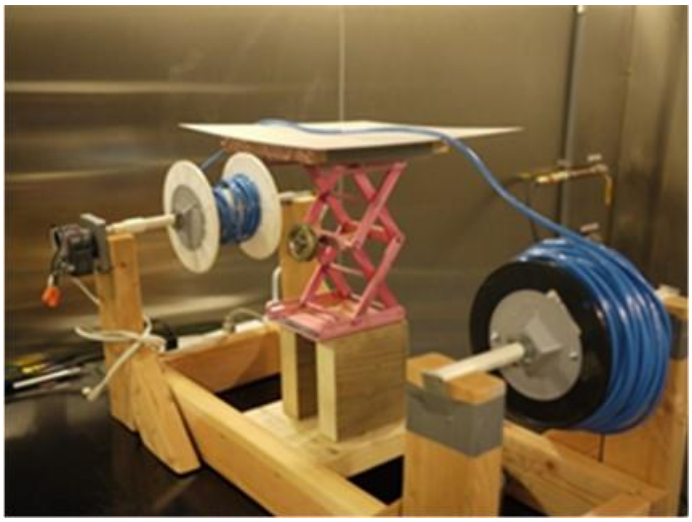


Figure 10: CAT 6 Cable Unwind Test Set up

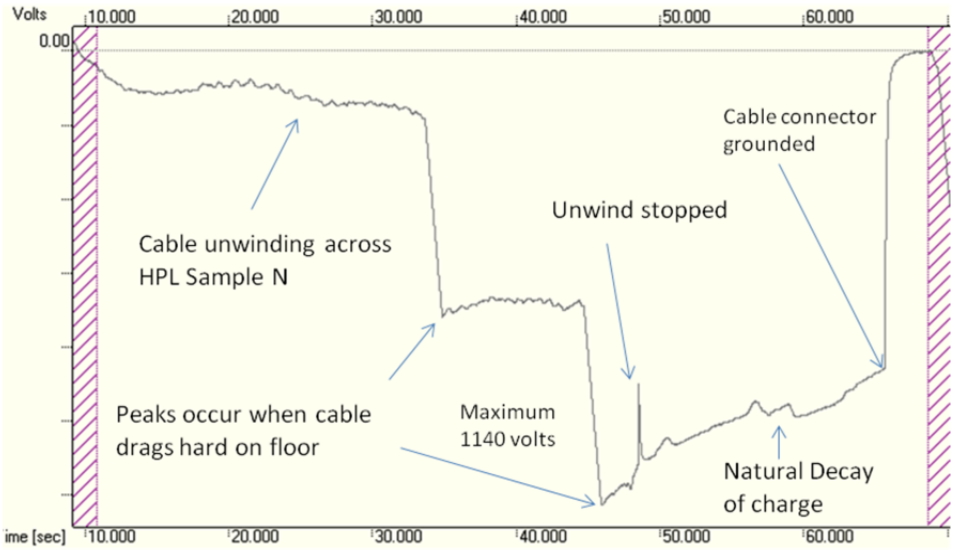


Figure 11: Voltage on the inner conductor of a CAT 6 cable during unwinding across a high-pressure laminate floor

1.4.3 LAN Cable Discharging Scenario

As shown in Figure 12, a typical LAN cable discharge situation includes: (1) Charged cable; (2) transformer possibly having common mode chokes included in an Ethernet connector; (3) PHY IC transceiver interface pins. The primary-side center tap of the magnetics is usually connected to a

Bob Smith termination circuit which consists of a resistor and a high voltage capacitor. During a LAN CDE, the discharge sequence, the Bob Smith circuit, the magnetic group and the PHY IC pin dynamic impedance will all affect the discharging scenario.

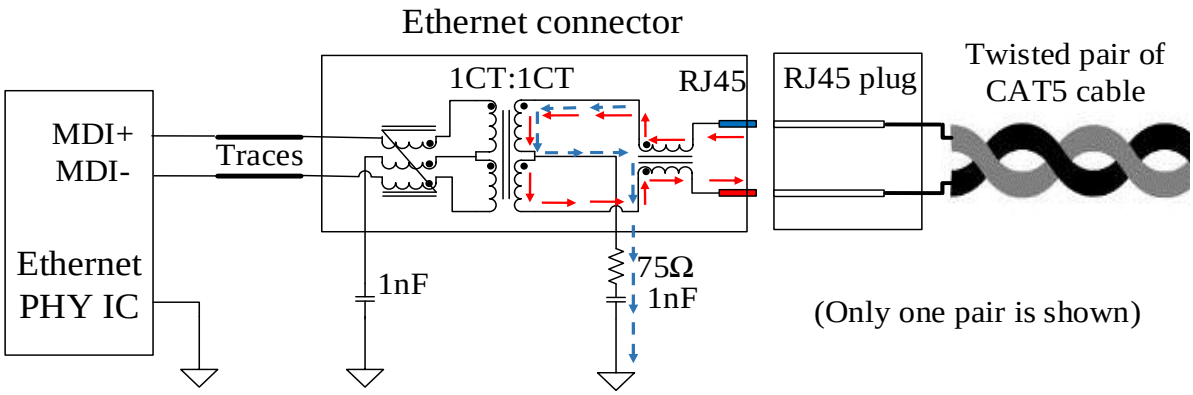


Figure 12: Schematic diagram of the LAN cable discharge situation. The system contains four pairs, here, only one pair is shown

When a charged LAN cable is plugged into an Ethernet LAN connector, not all pins make contact at the same time. One of the pins will spark over first. The first pin that contacts initiates a current flow between that wire and the LAN connector. Then, at least two different modes can be initiated by the second pin that mates. The second pin can either be from the same twisted pair, or from another twisted pair.

The assumption is that the LAN cable is charged in common mode. In other words, all 8 wires of the cable have the same potential with respect to a reference plane. When the first pin contacts, the discharge current flows via the common mode choke, and one half of the transformer primary winding to the Bob Smith termination circuit. The first pin discharge current path is illustrated by the blue arrows in Figure 12. This is referred to as a differential mode discharge, and the current magnitude mainly depends on the Bob Smith termination type, the common mode impedance the cable forms with respect to reference ground, and the charge voltage. Typical values for the resistor and the capacitor in the Bob Smith circuit are 75 Ω and 1 nF respectively, but other realizations are possible. For example, if power over Ethernet is provided, the capacitor value may be much larger. Furthermore, many center taps from different pairs or even cables may connect together and share the same termination circuit. This makes the first pin discharge current path become more complicated as multiple PHYs may be affected by one discharge.

If the second pin that mates is from the same twisted pair, the second pin discharge current path is illustrated by the red arrows in Figure 12. In this case, the current will flow through the transformer primary winding, and the first pin will be the main current return path. This is also referred to as a differential mode current.

As the discharge currents are in differential mode, the common mode chokes in the magnetic group cannot suppress the CDE currents. Differential mode discharge situations can occur under two circumstances:

- First contact causes a current flow from a pin, via the transformer, to the Bob Smith circuit
- If the first discharge caused a differential voltage on a pair (the analysis of this requires knowing the capacitance distribution between the wires, pairs and to ground) and the second pin that contacts is from the same pair, then a differential current will flow.

Most discharge currents will transfer to the PHY IC pins through the magnetics. The failure level of the PHY IC will depend on the magnetic module which are manufactured in several different configurations. Due to the large currents during an ESD event, nonlinear effects such as core saturation must be considered. The saturation of the magnetic cores can limit the amount of energy which is coupled into the transceiver circuit. In [Gan2016], the LAN CDE second pin discharge simulation result shows that the long pulses or high current levels will saturate the transformer, and this effectively reduces the PHY IC current, protecting the IC (see Figure 13).

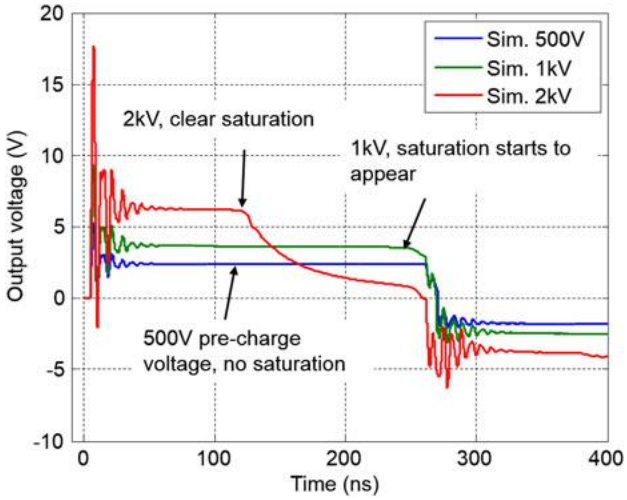


Figure 13: Voltage at the PHY IC pin side for a 25m long cable at different charge voltages [Gan2016].

1.5 Protecting Radio Frequency (RF) Antennas

With the increase of mobile and wireless applications, protection of the RF antenna ports from ESD becomes both critical and challenging. Antenna reception and signal integrity are important figures of merit for these products and virtually anything that is added to the circuit to protect it from ESD will impact its performance. Thus, considerable effort must be focused on either making the antenna self-protecting or minimizing the impact of the ESD protection elements.

One of the most common antennas in use for wireless applications is the planar inverted F antenna (PIFA). This antenna has a ground leg and thus can be inherently self-protecting. An example of a tunable PIFA antenna is shown in Figure 14.

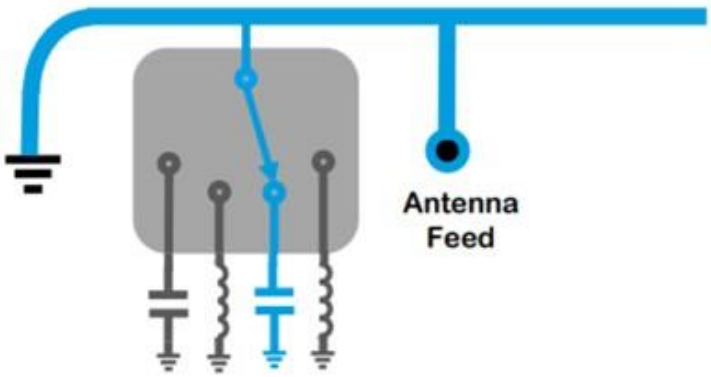


Figure 14: Tunable PIFA antennae

While the PIFA antenna is indeed grounded, care must be taken in designing the actual ground network. An antenna connected to a noisy analog ground will impact performance and can dramatically lower the antenna's performance. Thus, there is a tendency to design a DC ground that also provides some RF isolation. This is typically done by adding inductance in series with the ground connection. But this can defeat the purpose of an effective ESD ground. The Fourier transform of the initial peak in the IEC 61000-4-2 contact discharge pulse contains significant contribution from frequencies as a large as 1 GHz. Furthermore, there are additional high frequency components in the typical ESD gun pulse. Any inductance to ground in the PIFA antenna ground net will degrade the grounding of the high frequency components in the system level ESD pulse. Effective grounding of the antenna will require designing a ground net that provides some level of RF isolation as well as an effective ESD ground.

The second type of antenna in common use is the monopole antenna. This antenna tends to be higher performance than the PIFA antenna, but it is much more difficult to protect. An example of a tunable monopole antenna is shown in Figure 15. Since the antenna has no ground of its own, ESD protection design becomes critical.

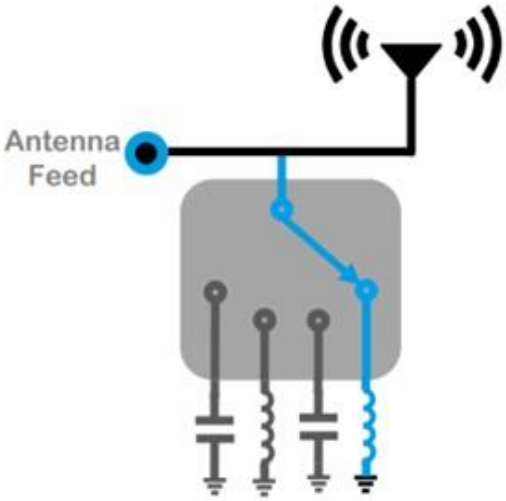


Figure 15: Tunable Monopole antennae

There is a tendency by companies that find the ESD protection of the antenna system challenging to push the requirements for ESD protection back on their component suppliers. This will lead to inefficient ESD designs since all the components connected to the antenna such as antenna switches, tuners, multiplexers, or other components must have their own protection. This not only duplicates ESD protection in the individual components, but it limits the ability of the system engineers from developing the most effective ESD protection that also minimally impacts performance. Ideally, the ESD protection of the antenna circuitry should be done at the system level so that there can be an efficient co-design of the ESD protection and RF performance circuit elements. With the development of ESD simulations at the system level through such approaches as SEED, the design of the RF antenna protection can be done much more intelligently.

Antenna ports that are external to the electronic component must, of course, be tested using the system level IEC 61000-4-2 test. For most wireless applications, including mobile phones, the device must pass Level 4 testing. Consequently, if the antenna is exposed, it will need to withstand 8 kilovolts contact discharge testing. For antennas that are not exposed, they need only be protected sufficiently to withstand the 15 kilovolts air discharge testing that is applied to the non-conductive exterior of the electronic device.

Chapter 2: Direct Pin Injection

Harald Gossner – Intel Corporation

2.1 Purpose of Direct Pin Injection of IEC 61000-4-2 Pulse

In real world stress situations IC pins are usually well shielded from ESD discharges. This includes mechanical design measures like pre-mate contacts of cable connectors, grounded shield metal of the connector and the chassis and electrical protection by filtering components on the PCB which mitigate the transient pulse on the PCB line towards the IC pin. Nevertheless, a partial stress, typically referred to as a residual pulse on the PCB line, can reach the IC component and cause damage or a malfunction. Also, an electromagnetic coupling can occur between the direct discharge path and nearby sensitive PCB paths.

Currently the direct discharge of an IEC 61000-4-2 pulse to a connector pin is excluded from IEC 61000-4-2 if a grounded shield is provided by the connector. However, as system design needs to consider the aspect of a residual pulse, it is industry practice that IEC 61000-4-2 pulses are applied to the connector pins even though IEC 61000-4-2 excludes this test. Since there is no specification of this test, performing this stress and the target values are largely differing. Primarily IEC 61000-4-2 ESD gun simulators are used due to the wide availability of the test equipment. Even if the waveform of the IEC 61000-4-2 spec does not match the waveform of the cable discharge, the practical experience of many generations of systems designs produced in high volume has shown that it provides a relevant test of the robustness in the field. This can be explained in that typically IEC 61000-4-2 failure mechanisms are dependent on the power or energy of the stress pulse and not on the details of the waveform. With increasing speed and downscaling of technologies a well-defined IC/PCB co-design is important to satisfy performance as well as robustness requirements. The essential base is the common understanding of the type of stress and the targeted stress levels by the IC and system design. **This requires a clear specification of the direct pin discharge to the connector pins.** The purpose of the chapter is to recommend a relevant and practical direct pin injection test at the system level.

2.2 Applying IEC 61000-4-2 Gun Pulses to IO Lines

Applying an IEC 61000-4-2 pulse to a connector pin using the commercially available ESD simulators poses various difficulties. To ensure a reproducible and well-defined discharge, a contact discharge to the pin under investigation should be performed. Due to the geometry of the connector pins with small distances and the large tip of the gun it can be difficult to impossible to contact a single pin (see Figure 16). In addition, the pins are often situated deeply inside the connector. A viable solution is a fan-out board with test pads of each line under test where the gun tip can reliably be contacted (see Figure 17). The board needs to have an appropriate jack to the connector and the board parasitics should be minimized.

Figure 16: Comparison of a USB-C connector Size and the Tip of an IEC 61000-4-2 gun

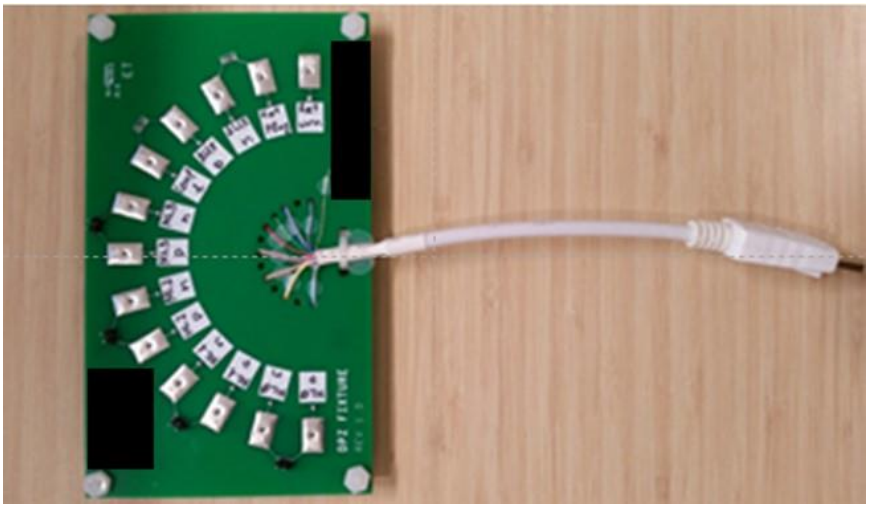


Figure 17: Example Fan-out Board used for Direct Pin Injection

As the PCB trace between the device pin and transient voltage suppression (TVS) diode acts as an inductor with efficient high frequency filtering in case of a low impedance state of the TVS diode, a 2-3 cm length of the PCB line between the branch point of the TVS diode and the IC pin landing pad is sufficient to block any overshoots related to fast transients in the first 5-10 ns of the residual pulse. Longer traces help to divert more current into the TVS path over the full pulse length. An example is given in Table 2. For the same IC component protected by the same TVS diode the direct pulse injection robustness can improve from < 1 kilovolt to 10 kilovolts when the trace length increases from 0 to 8 cm. While this can be a design optimization parameter for the form factor design, it needs to be considered for reference designs in order to avoid a too optimistic conclusion for a later form factor design with shorter trace lengths.

Table 2: Comparison between Different ESD Models

Trace length between TVS and IC pin	Current of first peak into IC pin	Current of second peak into IC pin
0 cm	11 A	6.5 A
2 cm	6.5 A	6 A
4 cm	No peak visible	6 A
8 cm	No peak visible	6 A

A direct pin stress of a fully assembled PCB, including all protection devices of the pin under test, enable applying the test procedures following IEC 61000-4-2. In the case of a partially dissembled board without a TVS diode the filtering of high frequency content of the IEC 61000-4-2 pulse by the PCB line is much less efficient. This can trigger failure mechanisms which are not apparent in a design using a TVS diode. To correlate the robustness against residual pulses a filtering of the 1st peak of the IEC 61000-4-2 pulse is recommended. This can be done using ferrites on the fan-out board (see Figure 18). In the resulting waveform the first peak of about 5 ns has vanished (see Figure 19).

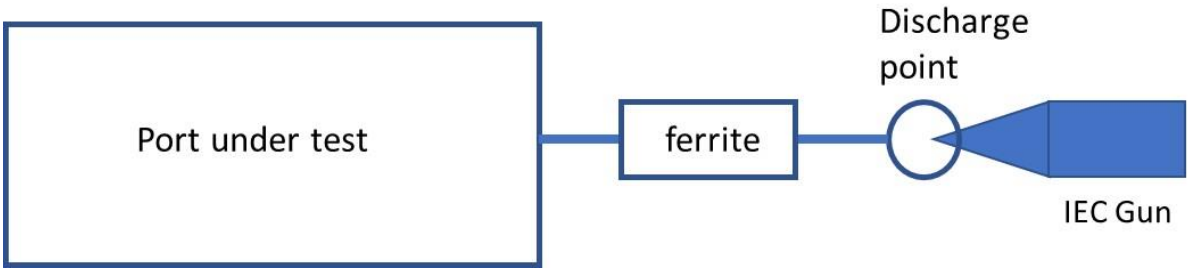


Figure 18: Set-up for IEC 61000-4-2 Direct Pin Discharge using a Ferrite for Fast Transient Suppression

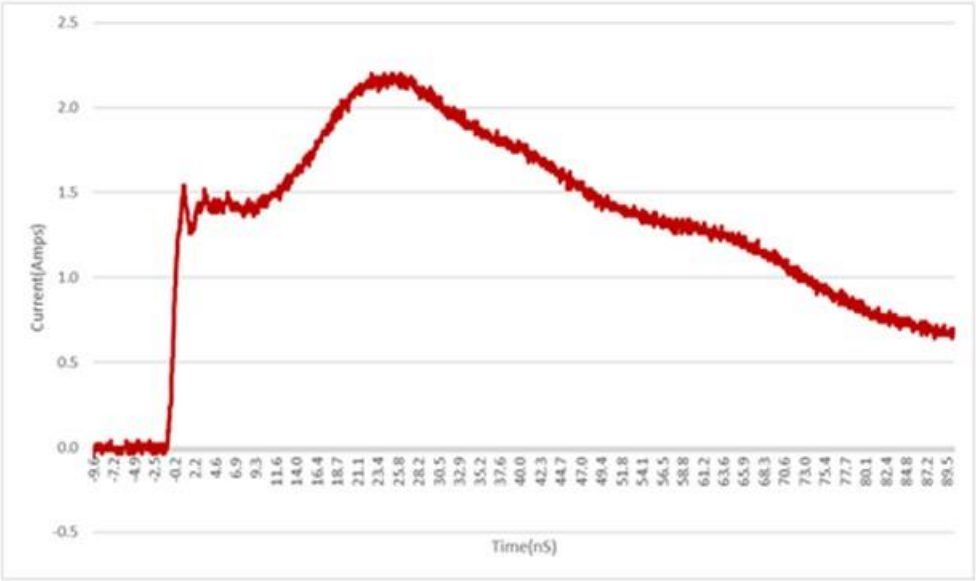


Figure 19: Discharge waveform into 2 Ohm of an IEC 61000-4-2 gun when a ferrite is mount near the discharge point. The first peak in the initial 1.2 ns has been attenuated

2.3 Transmission Line Pulsing

As an alternative waveform to an IEC 61000-4-2 ESD pulse, a trapezoidal transmission line pulse (TLP) can be used to characterize the ESD robustness. While this method has widely been used for characterizing IC pins, it has only been reported for a few applications on the system level. An obvious advantage is the similarity to the cable discharge waveform. In contrast to the IEC 61000-4-2 waveform, the TLP pulse enables varying the rise time and the pulse length over a wide range to explore the robustness of the pin or a TVS diode. TLP pulsing also provides a detailed analysis of the transient response of a semiconductor device to a fast transient, high current pulse. Additionally, the clamping behavior of the TVS devices can be extracted.

TLP testing will deliver the IV characteristic and the failure level by the same TLP testing procedure. It can be applied to an IC pin, TVS and discrete components as well as to the system port. An appropriate choice of the TLP pulse conditions is important to correlate to an IC pin and TVS diode behavior under IEC 61000-4-2 pulse conditions. Various TLP pulse length have been discussed in literature ranging from 30 ns to 100 ns. The longer pulse length leads to self-heating effects and to an increased differential resistance seen in the IV characteristics. With increasing pulse length, the power-to-fail level will drop as described by the Dwyer model [Dwy1990]. **A pulse length of 50 ns is recommended which leads to a good correlation of TLP failure current It2 to the hard failure threshold associated with the IEC 61000-4-2 second peak pulse current.** If the system port is stressed to emulate a cable discharge, the pulse length must be chosen following the discharge time of the selected cable. This can be estimated by the length of the cable and the speed of light which results in a value for the chosen pulse length of 14 ns/m as a rule of thumb. A recommended typical rise time is 1 ns, but in the case of extracting modelling parameters for transient turn-on of TVS diodes, various rise times should be used [John2011].

The use of needle probes for the purpose of TLP testing does have one advantage. Probes enable selecting the point of injection on the board in a flexible way, e.g. the probe can touch the soldering pins of the connector on the board avoiding the contact problem associated with the port pin inside a connector with a complex 3D geometry (see Figure 20).

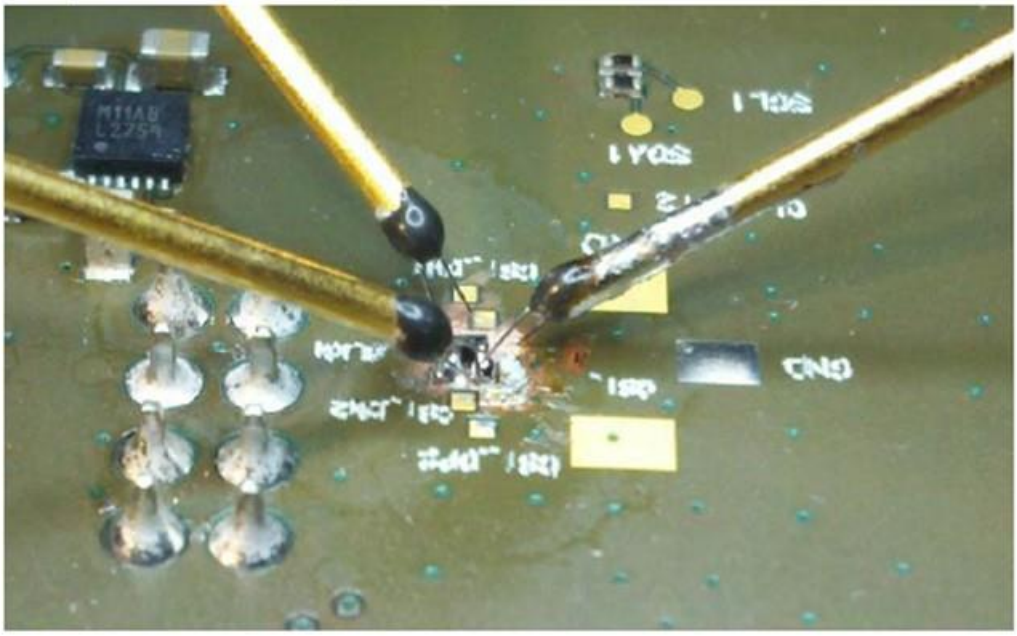


Figure 20: Use of needle probes to inject TLP pulses directly to the traces on the board. Voltage probes are added to sense the voltage drop.

2.4 Detection of Failure

A direct pin injection can result in various types of failure signatures. A fundamental distinction can be made between hard fails due to irreversible, physical damage and soft fails due to signal noise, power noise or latch-up, which are reversible. The latter leads to various categories of malfunctions described in IEC 61000-4-2. On the system level more severe soft fails can lead to a shutdown, a system hang, or battery drain and overheating due to latch-up.

In respect to the presented discussion, only hard fails are considered for the determination of the failure threshold of the system pin under test. This can be evaluated by leakage or impedance test of the pin and a subsequent functional test of the port interface. The functional test of the interface under test requires the removal of the stress test board or probe contacts and a connection to a client or host system or a loop-back test. Before the functional test a power cycling of the system is recommended to remove any malfunction of the system due to soft failures.

There are limitations in system level testing to detect minor physical damage in the IO. In particular, differential interfaces have low ohmic paths to ground making it difficult to detect small (in the microamp range) leakage paths. The interface might still be operating within specifications in the case of smaller damage levels. However, this can lead to a lifetime problem with an early fail of the system.

Chapter 3: Target Levels for Direct Pin Injection

Harald Gossner – Intel Corporation

3.1 Purpose

The definition of a target level for direct pin stress on IC pins supports the IC/PCB co-design approach for system efficient ESD design (SEED) protection. It opens a design window for the optimization of the system board protection. Knowledge of the target level for IC pin direct pin discharge and the target level of the system direct pin discharge allows the TVS vendors to develop appropriate TVS diode solutions.

3.2 Injection into IC Pin

The design window of the IC is determined by a destructive current level It2 and a destructive voltage level Vt2. In most designs, the required system pin robustness exceeds It2 of the IC and additional PCB protection circuit elements must be implemented matching the IC's protection design window. Vt2 provides an initial design window without considering the voltage drop on the PCB trace to the IC pin. Taking It2 into account increases the effective voltage design window for the TVS diode by adding resistance and impedance to the trace between TVS branch point and IC pin landing pad. With this knowledge a co-optimization with functional performance criteria can be performed.

The following recommendations address the **robustness of an IC pin (connected to an external port)**:

- A minimum It2 level of 2 amperes is recommended. This is extracted for a recommended TLP pulse length of 50 ns.
- The Vt2 window is set in relation to the maximum operational voltage VIOmax. The difference between Vt2 and VIOmax provides the useful design window. The recommendation is to maintain a minimum voltage delta Vt2-VIOmax > 4 V. This enables physically feasible TVS protection diodes with 0.3 Ohm on-resistance for high protection level at the port up to 8 kilovolts.
- To have a standardized and system relevant condition for the buffering cap between VCC and VSS it is recommended to attach a 1 µF cap with low serial impedance to the rails.
- To ensure a high robustness at all system power states, It2 and Vt2 should be extracted both for an unpowered domain and a powered domain at maximum VDD.

3.3 Injection into System Port

A direct pin discharge to the system pin of a reference design serves the purpose of proving feasibility of a protection concept. The testing of the final form factor design should provide the confidence to deliver a robust design to the market.

The following recommendations address the **robustness of a system pin**:

- The target level is ultimately a topic of the supplier-customer negotiation. There is system specific knowledge with most of the system designers.
- The following guidance can be used: a reasonable maximum requirement to pins of a cable connector is the required IEC 61000-4-2 level to the metallic parts of a system. A typical value is 8 kilovolts contact discharge. However, more recent investigations of USB cable discharges indicate that a level of 2 kilovolts would be sufficiently robust for USB cables fulfilling the standard shielding requirements [Stad2017]. Avoiding excessive target levels helps to balance performance, cost, and area.
- A reliable system pin test requires a fan-out board to guarantee a reproducible contact discharge.
- All relevant power states should be investigated.

Chapter 4: ESD Generator Modelling

Sen Yang, MS&T EMC laboratory

4.0 Introduction

The purpose of this chapter is to compare the different ESD generator models used for system level ESD simulations. The average measured value of peak current and rise time for each load impedance from Chapter 7, Section 7.1.2 were used as reference values in this chapter. For SEED simulations of direct pin-related contact discharge, SPICE based models are most suitable, but there is a wide range of SPICE based models to choose from. In this chapter, differences between the models and their impact on discharge scenarios into a load are discussed.

4.1 Current Source Models

Several authors [Wu2013, Kat2010, Yua2006, Son2003 and Fot2006] have introduced mathematical descriptions of current source models for an IEC 61000-4-2 gun discharge. As these models do not include any output impedance of the ESD generator, they might fall short in the prediction of currents for non-shorted circuit loads. Others have also proposed models for International Organization of Standards (ISO) 10605 pulses [Mer2012].

The main current source model for system level ESD generators is given in the IEC 61000-4-2 standard. The waveform describes an idealized contact mode discharge waveform. The waveform is somewhat related to observed human-metal discharges. However, most human-metal discharge measurements do not report such a clearly distinguished second peak after the initial peak. Here the IEC 61000-4-2 waveform deviates from most measurements of human metal discharge and the clearly double peak structure of the IEC 61000-4-2 waveform must be better understood from a legacy perspective. Changing the waveform to a waveform that closely resembles the measured human-metal discharge waveforms would require changes to all existing ESD generators.

A current source model into a short provides misleading results if the model is applied to situations in which the DUT is small and non-grounded. Such DUTs (for example, a cell phone) form a capacitance to ground or to the horizontal coupling plane (HCP). If a current is forced which equals the IEC 61000-4-2 waveform, then the small capacitance of such a device may be charged to a voltage much higher than the initial charging voltage. Forced current source models must be handled with care for all situations except a discharge through a short.

On the other hand, authors like Wang et al. [Wan2013b] and Zhou et al. [Zhou2014] proposed equivalent circuit models that are derived from the mathematical equations of the IEC 61000-4-2 standard waveform or from measured contact mode currents. Figures 21 and 22 are the equivalent circuits for the Zhou et al. model and Wang et al. model, respectively. These models can be more relevant for a broader range of loads.

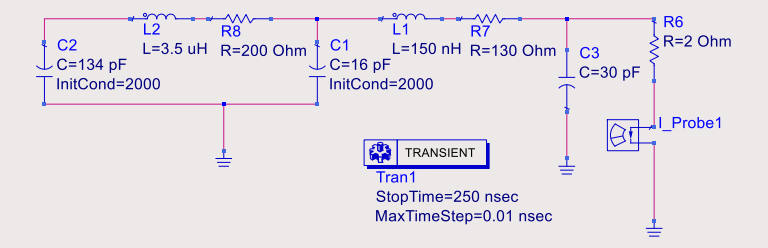


Figure 21: Zhou et al. model [Zhou2014].

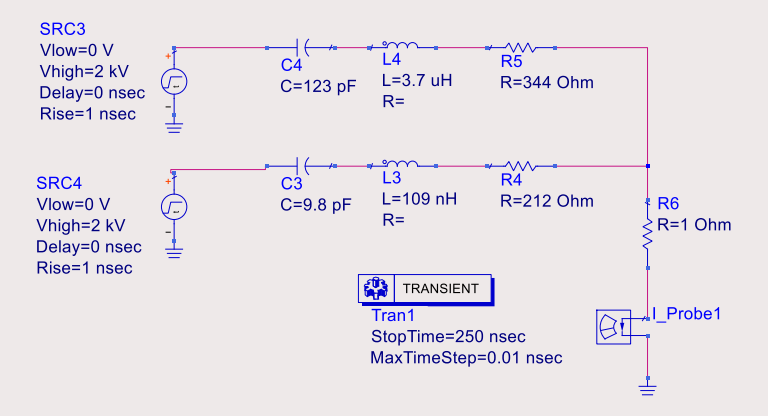


Figure 22: Wang et al. model [Wan2013b].

4.1.1 Physical-based Models

A physical-based model uses components to describe actual structures or components of the ESD generator. For example, the main resistor capacitor network (RC) constant is obviously expressed as the RC component block, but the ground strap's inductance can be explained as an inductance (Figure 24, Figure 27, and Figure 28) or a transmission line (Figures 25 and 26). Further, the excitation of the ESD generators can be expressed by low pass filtering a voltage source which rises in < 500 ps (which is closer to describing the voltage collapse in the relay) or by a slowly (e.g., 1 ns) rising voltage source (Figure 25); i.e., avoiding any representation of the relay and associated low pass networks. The coupling from the body of the ESD generator to the surrounding is often expressed as an RLC component block (Figure 24 to Figure 28). The following figures (Figures 23 to 28) represent different ESD generator circuit models.

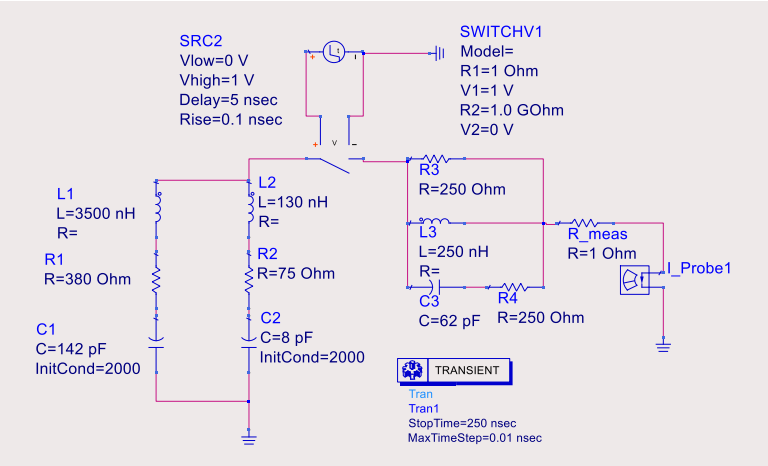


Figure 23: Tamminen model [Tam2016].

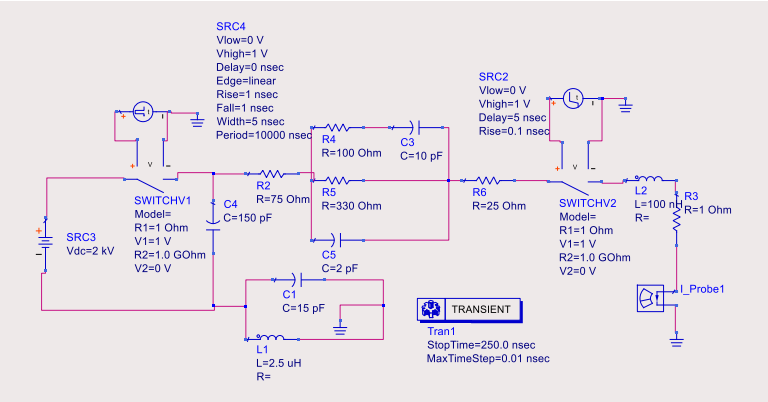


Figure 24: Notermans model [Not2016].

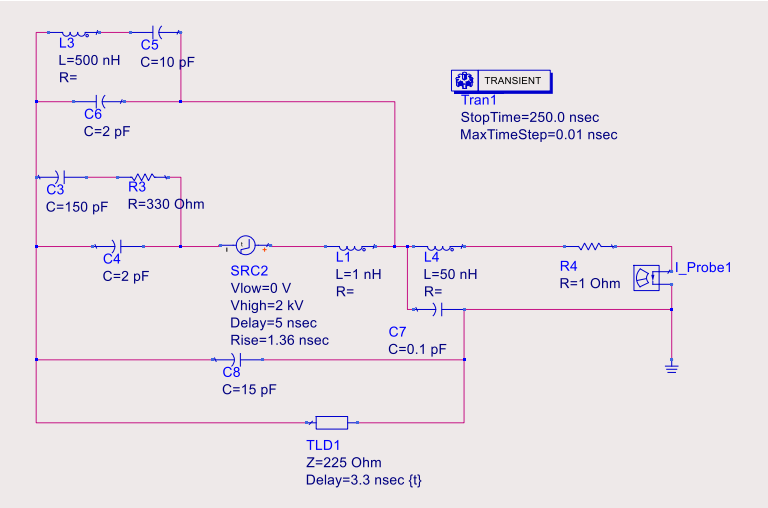


Figure 25: Sekine model [Sek2013].

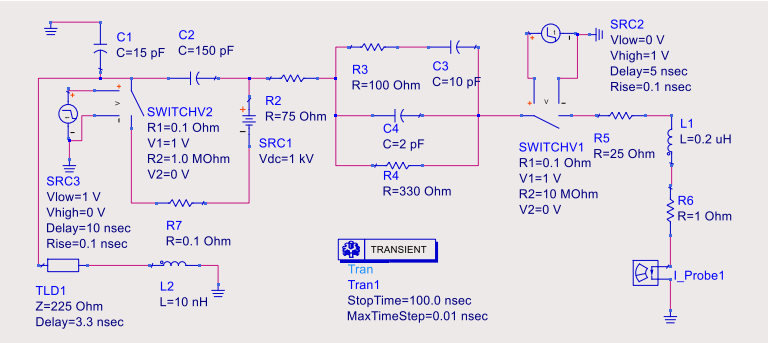


Figure 26: Caniggia model [Can2006a].

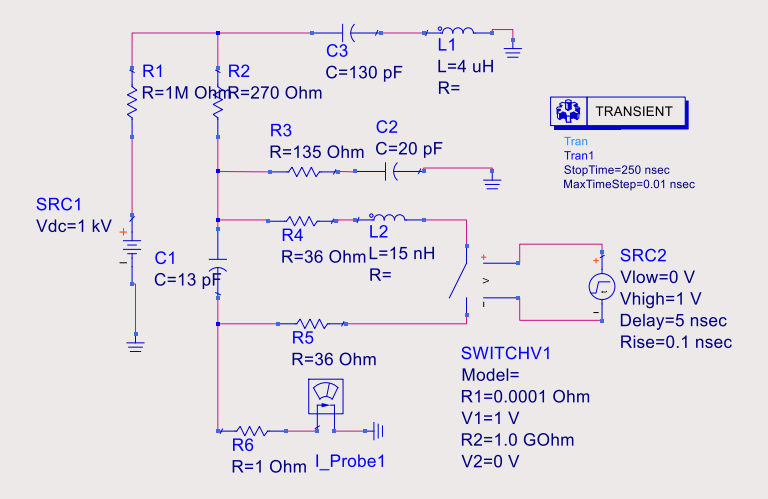


Figure 27: MST model [Wan2003][Li2015].

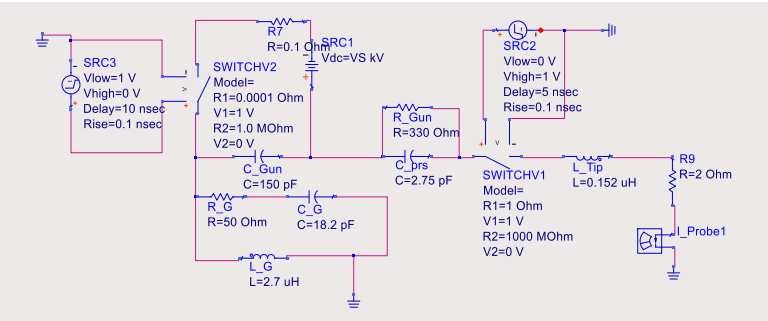


Figure 28: Yousef et al. model [You2017].

4.1.2 Simulation Results

As a first step, the current waveforms for discharge into a short are simulated using PathWave Advanced Design System (ADS) and shown over the entire time frame and over the first 7 ns (Figure 29). As shown in Figure 29, the Zhou et al. model has a peak value of 9.62 amperes, which is 28.3% larger than the IEC 61000-4-2 specification of 7.5 amperes. Furthermore, the simulation of different load impedances also shows that the Zhou et al. model deviates strongly from the

measurement results and other models. Thus, it was excluded in the analysis of the effect of load impedances. The simulation results from the models are summarized in Table 2 with respect to the specifications of the IEC 61000-4-2 standard.

Table 2: Comparison of 2 kV peak values and rise times, data that violates the IEC 61000-4-2 specification is shown in red.

Model	1st peak current [A]	10%-90% rise time [ns]	30 ns current [A]	60 ns current [A]
Caniggia	7.04	0.94	2.49	1.81
Notermans	8.26	0.56	4.04	1.76
Wang et al.	7.23	0.94	4.00	1.97
MST	7.17	0.81	4.14	2.37
Tamminen	7.66	0.75	3.86	2.24
Sekine	7.46	0.91	2.32	2.52
Zhou et al.	9.62	1.04	4.40	2.36
Yousaf et al.	7.57	0.67	4.93	2.31

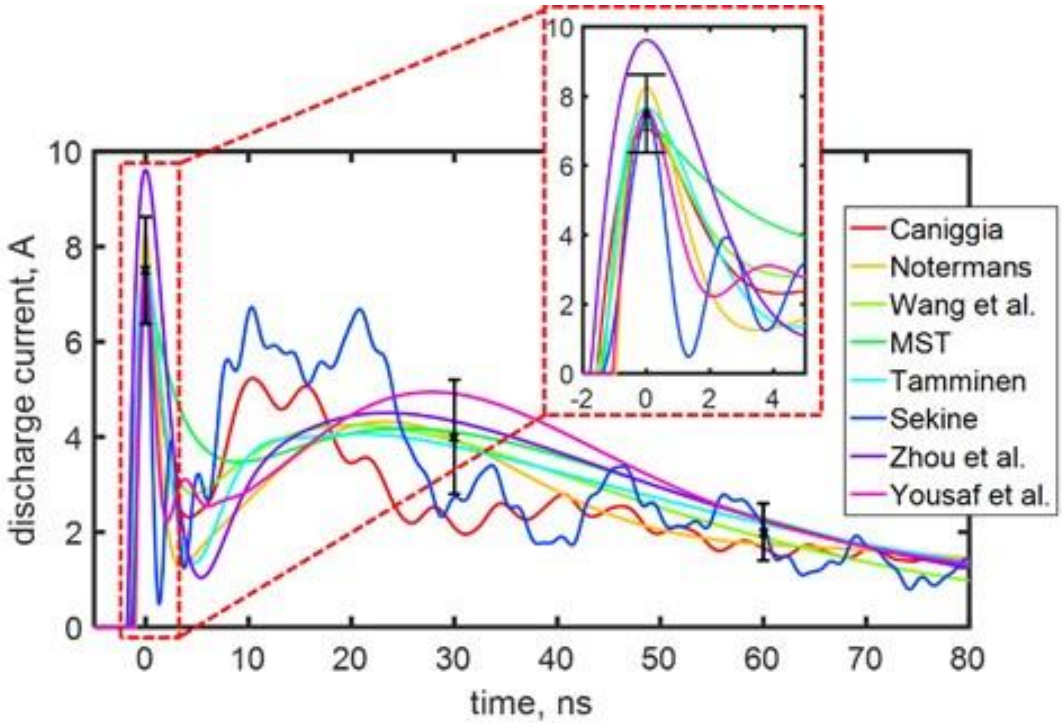


Figure 29: Simulated currents for discharges into a short at 2 kV. Waveforms are time shifted to arrange the maxima at 0 ns. Error bars indicate the IEC 61000-4-2 limits.

Two models, the Caniggia model (Figure 26) and the Sekine model (Figure 25) introduced transmission lines instead of inductances for the ground strap. Ringing in the waveforms of actual ESD generators can sometimes be attributed to the length of the ground strap. If the ground strap is parallel to a conducting surface [Can2006b], it forms a low loss transmission line. The transmission line causes ringing within the tail of the waveform, which may cause the current values for 30 ns and 60 ns to fall out of the allowed tolerance of the IEC 61000-4-2 specifications. However, after replacing the transmission line with an inductance of about 2 µH, the current waveform tail is within the tolerance. In the case where the ground strap forms a triangular shape, as the calibration set-up describes [Wang2003], it will radiate above 100 MHz, leading to little ringing.

The next step is to compare the models for different load impedances. Here, a set of loads is selected that matches the ESD target loads used in the ESD generator measurement in the previous section.

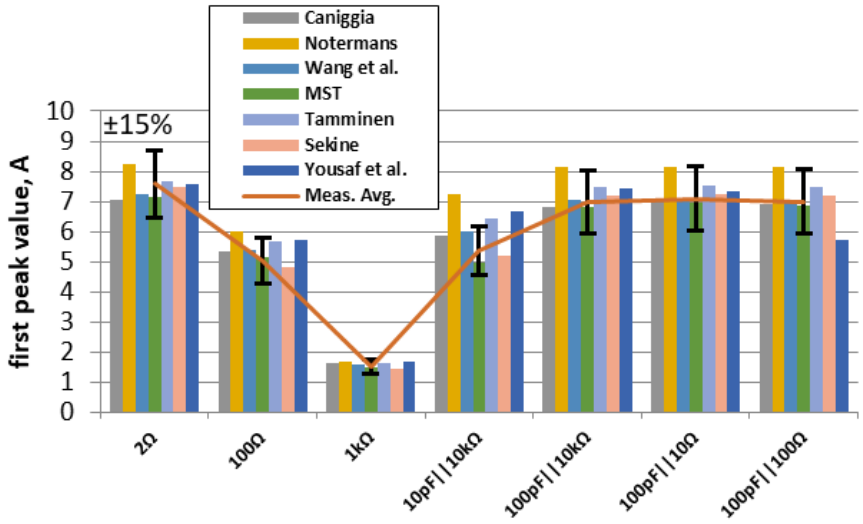


Figure 30: First peak values for different ESD generator models. The error bars indicate ±15% variation of average measured values.

The peak values are shown in Figure 30. For all models, the peak value for a 2 Ω load is very close to the average measured peak value which again is in good agreement with the IEC 61000-4-2 standard's current specification (3.75 A/kV). All modeled and measured waveforms show a similar tendency for discharges into other loads. This indicates that the "output impedance" of these models is rather similar and not far away from the measured data.

The rise times are shown in Figure 31. Significant differences are observed for the 1 kΩ load. Only the MST model and Wang et al. model's rise times are within the range of measured rise times for all load impedances (variation ± 25 % of average measured values).

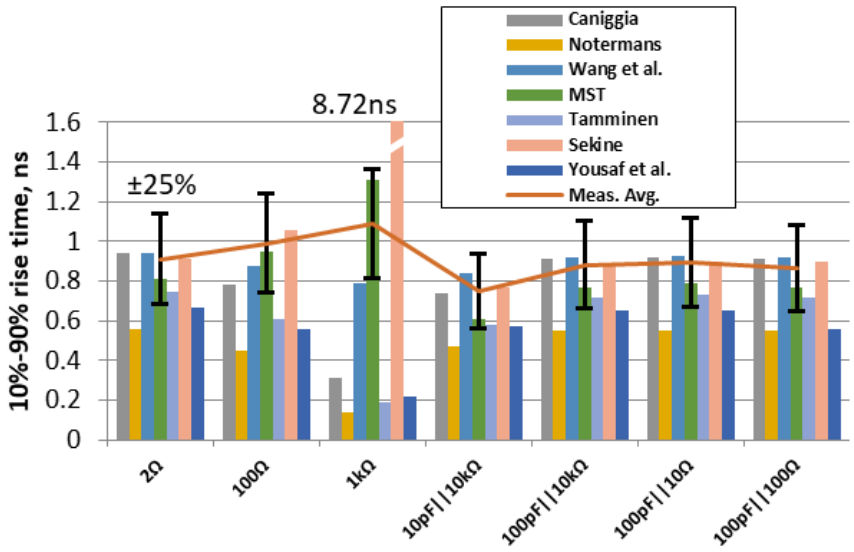


Figure 31: Bar diagram of 10%-90% rise time of the first pulse (Unit: ns). Note: the y-axis is limited to 1.6 ns for better comparison, all though the Sekine model rise time is 8.72 ns. The error bars indicate ±25% variation of average measured values. The IEC 61000-4-2 standard (2008) allows for +/- 25% variation around 800 ps for discharges into a 2 Ohm target in contact mode.

4.1.3 Discussion

As a SEED design is based on SPICE models, a similar question can be raised for simulation models: do these models predict the behavior observed in measurements for different load impedances? Or are there any models which strongly deviate from the behavior observed in experiments? Most ESD generator SPICE models have the first peak values close to the measurement of a real ESD generator. However, a pronounced difference is observed for the rise time in the case of a 1 kΩ load. Only two models, the MST model and the Wang et al. model yield the rise time which is within the range of 0.7-1.2 ns for all load impedance conditions simulated. The MST model is a physical model which means that it represents some details of a real ESD gun. On the other hand, the Wang et al. model is a waveform-based model, which is derived from mathematical approximation of the IEC 61000-4-2 standard waveform. Both models performed well when loaded by impedances other than a short.

4.1.4 Conclusion

The simulation result of the ESD models considered here (except the Zhou et al. model) agree well with the IEC 61000-4-2 standard (2 kilovolts, 2 Ω load), for both peak values and rise times. The peak values for all models are close to the measurement results in each load impedance scenario. On the other hand, pronounced differences are observed in the rise times in various load impedance conditions compared to the real ESD generator results. Further, some models such as Noterman and Yousuaf et al don't meet the tolerance of 15%. All the other models can provide rise times around 1 ns for all load impedances except for the special case of 1 kΩ where only the MST and Wang et al. models comply with the measurements.

Chapter 5: Impact on PCB Protection Design

Jeff Dunnihoo, Pragma Design

5.0 Introduction

Notwithstanding explicit directives and reasonable opinions on both sides regarding the merits of striking pins directly on external system connectors, the problem exists for the designer as to what should be done when the IEC 61000-4-2 qualification tests fail for that port.

Hard errors may create physical damage which clearly indicates the beginning point for the investigation of improved robustness. However, the failing device is not necessarily the problem to be addressed, nor is it always an option.

For example, when a high definition multimedia interface (HDMI) application specific integrated circuit (ASIC) fails during system ESD testing but the transient voltage suppression (TVS) protection remains undamaged, the designer needs to (quickly) design an improved protection strategy to protect the HDMI ASIC. The designer probably has no immediate pin-compatible device available to replace the HDMI ASIC, therefore a SEED analysis may be necessary to determine a better TVS option and/or other shielding, layout, or other mitigation strategies.

The case might be made that the test condition or level is too severe, according to the old adage about the patient complaining to the doctor, “Doctor, it hurts when I do this.” To which the doctor replies, “Then don’t do that.”

But what of the condition where other systems (or worse, competing systems) have passed this onerous and “unfair” test condition? In this case the designer really has little choice but to try to improve the system robustness which has been a tedious job of trial and error in the qualification lab but has recently been alleviated by advances in simulation techniques.

5.1 SEED Concept and Impact of Interface Specific IEC 61000-4-2 Targets

SPICE-based simulations typically assume that the circuit will remain “functional” during a transient analysis. The nature of ESD and electrical overstress (EOS) suggests that normal operating conditions of the devices will be exceeded during the analysis, and this means that the dynamic response of devices is not only modulated by currents, voltages and time, but that the devices change their response based on recent abuse. What happens when the devices are taken far beyond their operating boundaries for short periods of time is a critical consideration. Sometimes it is enough to know that one or more devices have failed, and that is that. In some cases, it is interesting to know if a device will “fail open” or “fail short” and though damaged and more vulnerable, if the interface may still operate after the destruction.

First order protection circuit design analysis is often based on datasheet parameters of TVS devices, such as ESD rating (target IEC 61000-4-2 robustness rating, etc.), and clamping voltage, etc. These

parameters are usually tested under the one condition which they will never see in a circuit; by themselves!

Since TVS devices are always included in a circuit to divert strike current away from the device under protection (DUP), the actual clamping voltages at the two devices are distinct and the voltage at the protected device during a strike is not zero. The current diverted by the TVS is not 100 %, and the residual current into the protected device is also not 0 %.

Second order modeling of this interaction comprehends the Kirchhoff current division between these two dynamic devices, and the current, voltage, power and energy maximum limits which can cause latent or permanent damage in either the TVS or DUP (or even the PCB traces themselves if the pulses are sufficiently energetic.) Most device input/output buffer information specification (IBIS) or SPICE models available today provide information about "clamping devices" in device IOs, but these elements were intended to model signal integrity issues like overshoot and ringing within 5-10% above and below VDD and VSS. ESD/EOS strikes inject levels 1000x or more than what are contemplated in those models, and while simulators will happily extrapolate those models out to +/- 50 amperes peak for a 4 mA clamp, there is no information on when the device will fail and how it will behave on the way there and beyond. In the framework of SEED this led to the introduction of high current models for behavior of IO pins as well as TVS diodes [InCWP3PI]. SEED models are applicable to short pulse currents up to several tens of amperes. They need to account for package as well as IO circuit behavior and should flexibly be used for various simulators like Spectre, ADS, and SPICE simulators [ESDATR26].

Given meaningful device models in the ESD/EOS regime, this level of approximation provides superior estimations of the system level robustness for a given conducted pulse applied to a given node for the specific devices. However, it does not typically address soft errors, system upsets, secondary discharges or coupled pulses into adjacent conductors and devices.

Third order modeling attempts to virtualize the entire 3D system assembly and solve the aggressor E- and B-field interactions predicted by Maxwell's equations. Given the exorbitant amount of accurate physical and electrical model input required, this can theoretically provide the most complete and accurate representation of an ESD/EOS strike on a system. It is also extremely difficult and time consuming. While elegant and expensive, 3D field-solvers are commercially available and extremely powerful, given the dearth of accurate ESD-regime electrical models for devices, they can also produce prodigious amounts of "Garbage-In, Garbage-Out" results.

For most quantitative "compare and contrast" analysis, though, the second order modeling as discussed above, with validated models, can provide excellent results for "better or worse" decisions.

For example, the simulation in Figure 32 (red line) analyzes a system ASIC failing with a "zero Ohm jumper" resistor between the TVS and its GPIO input. Selecting a 2 Ohm resistor instead that also doesn't affect the I/O operation reduces the residual ESD current by almost half. Further testing is thus warranted to ascertain if the system can then pass the target ESD qualification level in the lab with potentially only a BOM change and no additional cost.

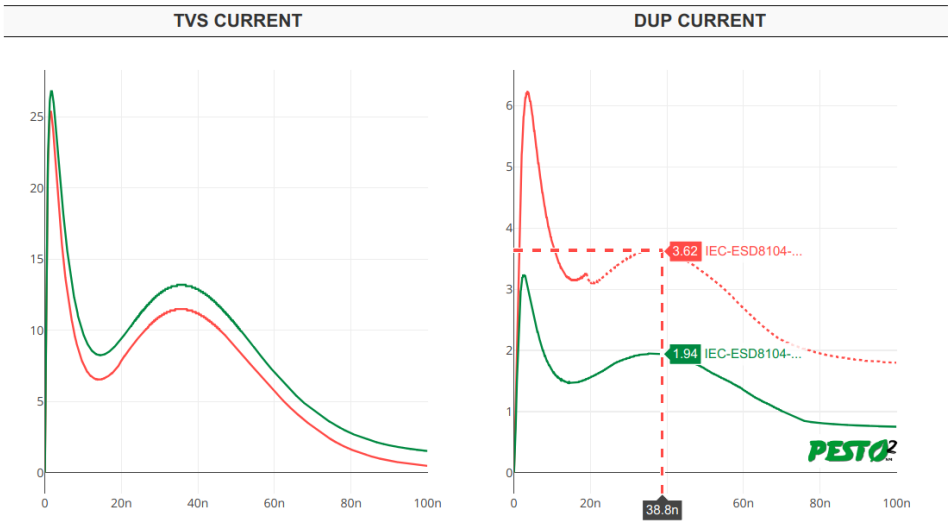


Figure 32: TVS clamp current at 8 kV IEC 61000-4-2 left, ASIC GPIO residual current right, “zero Ohm jumper” in red, 2 Ohm resistor in green.

5.2 Limits of Simulation

Of course, no simulation under any circumstance should be assumed to answer all questions, nor be extrapolated outside its limited sphere of valid inputs. The pass/fail criteria of a system are defined at the system level. For example, one TVS device may clamp to a lower voltage and faster than another device. This additional shunt current may inject undesirable currents and rise times into power rails or ground, causing secondary upsets on other devices.

5.3 Direct Pin Currents

5.3.1 Reasoning for Pin Specific Stress

Generally, it is assumed that connector shielding precludes direct strikes, and therefore pins should not be subjected to ESD testing for characterization. Below are several cases where direct and indirect stress can be applied to an “external” line exposed to the outside world.

1) When a line is exposed at the opposite end of an attached cable. Even when a peripheral such as a mouse or thumb drive is attached without a connection related event, a device may expose a path via plastic housing joints or button/LED entrance, etc.
2) Sequenced connection related (CDE) events
3) GND/shield pulses inducing current into adjacent signal lines.
4) Actual zaps to connector pins are possible, even when most discharges prefer shields (as seen in this multi-zap overlay at 20 kilovolts in Figure 33).
5) In specific applications where there is no shielding at all, such as an automotive or ethernet environment.

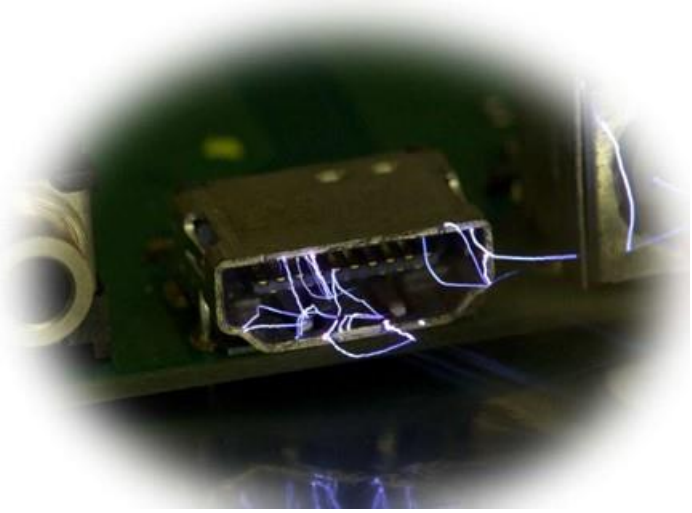


Figure 33: Multi-zap Overlay at 20 kV

5.3.2 Interface Types (USB, HDMI, Ethernet, audio, antenna, etc.)

There is an extended set of application specific interfaces which are exposed to system ESD discharge energy and need to be protected by TVS devices, see Table 3.

Table 3: Examples of interface type exposed to IEC 61000-4-2 ESD stress pulse energy for various applications.

Automotive	Wireless	Wireline
Controller area network (CAN) Bus	Antenna Port	A/B Line Driver
LIN Bus	USB Interface	Ethernet
Camera Interface	Camera Interface	HDMI
Display Interface	Touchscreen Interface	Display Port
USB Interface	Headset	eSata
Sim Card Interface	Sim Card Interface	

5.4 SEED Pass Criteria

Given that the residual pulse that a protected device sees from an air- or contact-discharge will be substantially modified, attenuated and morphed from the reference IEC 61000-4-2 calibration waveform, the failure mechanism may be dramatically affected for a given device, depending on what kind of protection is placed in front of it.

It is not possible to generalize a single static failure level in one parameter (such as peak current) that will properly indicate damage (or potential soft failure in some cases) under all stressors. However, physics-based models for current-and-time (fusing) and power-and-time or energy may often come close to approximating more than one particular failure mode for more generalized stressors.

In practical terms of guiding a useful design decision for a matching PCB design which can successfully protect the connected pin, model parameters such as peak failure currents (and others as mentioned above) for various pulse durations can be defined. These failure criteria characterize the robustness of the specific pin under consideration from the chip-level perspective [ESDATR26] However, that failure criteria may be completely unrelated or uncorrelated to the more general system level testing failure criteria. Pin level failure models may be defined by a specification limit guard banded to guarantee, for example, a defined leakage limit caused by ESD damage across process and temperature. ESD currents injected in this example that exceed the model's limit may cause a slight increase in leakage, but this might not actually affect operation in any detectable way during IEC 61000-4-2 testing.

In most cases, the actual measured robustness for a limited test sample will perform better than the worst-case, guard-banded specification guarantees. Designers at the chip and system level must both fully communicate and consider the likely divergence in robustness testing and simulation due to the selection, type and guard-banding of system and chip-level failure criteria.

5.5 Soft Fail SEED

Even while using an IEC 61000-4-2 ESD gun that is fully compliant very different pass and fail levels can be found depending on the brand of the gun, the set-up of the stress experiment and even the operational mode and conditions of the system.

In most cases a difference is seen in soft fails, but also a variation of the hard fail threshold can be observed. Reasons for uncertainties in the test results are discussed in previous chapters and improvement measures are proposed. But a soft failure, where an ESD direct pin injection, or EMI-coupled noise event causes a system signal or data corruption state that is detectable as an ESD-induced failure criteria is exceptionally difficult to simulate due to the complexity of the software and hardware functionality to be simulated.
It is possible, however, to simplify the failure criteria to a worst-case window and evaluate protection options again with the SEED approach.

For example, suppose a -500-mV glitch on an exposed signal line of at least 1ns in width is known or observed to cause a system upset. This might be due to a corrupted state machine or triggering on chip protection in a non-damaging way. This pulse might require rare alignment and timing to make the upset occur (thus the multiple strikes replicating real-world pulses described in Chapter 8 are also important to help catch a system in just the right timing to cause an upset.) Assuming that a large number of zaps allow this condition to be observed in the real world, albeit intermittently, we can assume that the prudent design strategy is to assume that "if this vulnerability can happen, it will happen and at the worst possible time." (Murphy's Law applies.)

Thus the SEED failure criteria may utilize the same direct pin injection simulation as for hard-failures, but instead of grading the pass/fail result by a damaging It2 level or other energy related failure, the simulation may rely on a signal integrity limit signature such as the glitch example above. If that envelope is exceeded during a simulation, it may be useful in predicting a possible failure in IEC 61000-4-2 gun testing.

With so many variabilities affecting test results, it may not be possible to encapsulate all the situations in a complete test suite. However, certainly when comparing multiple ESD mitigation or protection component options in the same circuit, a relative susceptibility to a soft-error may be weighed reasonably with this approach. Here again, SEED simulation can provide advantages for the designer even with soft-failures.

5.6 Conclusions and Correlations

When a system fails IEC 61000-4-2 qualification testing, the designer is tasked with identifying the unexpected susceptibilities and vulnerabilities that were exposed via gun testing. Many simulation and analysis tools are now available, and the designer can extract information about the system design and components. However, part of the overall qualification system as defined by IEC 61000-4-2 is not necessarily as easily represented in even the most elementary testing situations due to anomalies detailed elsewhere in this paper. The more reliably and rigorously refined the IEC 61000-4-2 test is, and the more repeatable gun testing results are, the more readily predictions and "first time right" design decisions will lead to robust, cost-effective and ***passing*** systems.

Part B: Discharge to Chassis and Display

Part A of this WP focused on discharges to pins. Part B takes the complete chassis into account and derives suggestions for improved IEC 61000-4-2 testing. Here the goal is to improve the repeatability of test results and to provide guidance for meaningful testing. This is partially done by the analysis of existing problems in the testing, and partially directly formulated for implementation in test laboratories.

Chapter 6: Historical Problems Observed when using the IEC 61000-4-2 Standard

Dr. David Pommerenke, Graz University of Technology

6.0 Motivation: High Test Result Uncertainty of System Level ESD Testing

ESD testing in accordance to IEC 61000-4-2 or derived standards has a high-test result uncertainty. Soft failures are especially hard to reproduce. Multiple reasons contribute to this difficult situation.

The present method of calibrating ESD generators covers the voltage and the discharge current in contact mode into a large ground plane (with the ESD generator held perpendicular to the plane) . From this, it is possible to determine the calibration uncertainty. The calibration uncertainty [Leu2001, Sro2003, Jan2010, Bar2008, Bar2010 & Mor2011] analyzes the effect of oscilloscope bandwidth, ESD target used and cables on the contact mode short circuit discharge current calibration.

These papers point at small effects of the calibration chain on the current or the voltage displayed by the oscilloscope. However, the differences caused by calibration test setups are insufficient to explain the test result variations observed in multiple test laboratories. Variation of soft-failure test results in which different manufacturer's ESD generators are used, often reach 1:2 (expressed in fail voltage levels) and may reach 1:3 [Koo2008]. Neither the uncertainty of the current waveform test results, nor the variations of the waveforms (there is no specification on the waveform, but only a specification on 4 parameters) can explain the large variations in the observed test results.

Consequently, improving the calibration of the contact mode discharge current cannot reduce these test result variations.

The test result variation is caused by a wide range of effects, not all of them related to the ESD generator itself. The dominating reason for soft-failure level variations, caused by changing the ESD generator brand, is due to the differing transient fields of the various ESD generator brands. This is an unintended consequence of using an ESD generator when running ESD testing. However, there are also many other contributing factors.

Parameters that contribute to the large test result uncertainty are:

- The transient field of ESD generators varies strongly from brand to brand

- No air discharge specifications, consequently, there are larger differences between generators in air discharge compared to contact mode
- Repeatability of air discharges due to natural variations in the spark length
- Pre- and Post-pulses
- Micro-amp pre currents due to field emission currents in the relay prior to the discharge
- No contact mode current specification into loads other than a short, this is especially important for discharges into small, not directly grounded DUTs
- Insufficient number of ESD pulses applied to each test point to have a statistical meaningful result considering time varying sensitivities of DUTs
- Testing at a level, such as 4 kilovolts, but not determining the failure threshold. To illustrate this, consider a case in which the actual failure level would be at 4.1 kilovolts. It would pass 4.0 kilovolts. But even small uncertainties would show the DUT passing in some labs and failing in other labs. Testing should be done to levels significantly above the limit such as to at least 6-8 kilovolts.
- Test point selection
- Not recognizing that secondary ESD has occurred (secondary ESD is when one part of a system under test becomes charged and then discharges to another part of the system)

6.1 Test Result Uncertainties

6.1.1 Importance of Air Discharge as a Mandatory Test

The majority of real world ESD events are air discharges. Most of the approaches of charged humans or objects will be toward plastic enclosures, screens, and connectors. These approaches may lead to (a) a discharge with sparking, (b) a corona surface discharge which has no visible sparking, but still may disturb or damage, e.g. a display, or (c) no relevant effect. Air discharge is the largest threat in the field. Testing according to the IEC 61000-4-2 standard should address this. In the maintenance cycle of the IEC 61000-4-2 standard the maintenance group MT-12 has suggested to remove air discharge from the mandatory testing requirements. However, the Industry Council on ESD Target Levels considers air discharge as a relevant and necessary system ESD test and proposes approaches to improve repeatability of the test.

By removing air discharge testing from the mandatory testing requirements, discharges to systems with plastic enclosures and displays could become an optional testing routine leading to coverage gaps in the system qualification. As most portable enclosures are made from plastic, and since those enclosures are especially prone to receiving ESD events, a large increase in devices susceptible to field failures would be expected.

This white paper describes several crucial steps to improve test result uncertainty, including the documentation of discharge currents during the ESD testing and a better calibration method for air discharge.

6.1.2 Air Discharge – Variation due to Arc Length and Approach Speed

A challenge in today's IEC 61000-4-2 testing is that air discharge current waveforms are not very repeatable. This is mainly due to the physics of the spark formation which strongly depends on ambient conditions as well as the test equipment and its operation. Even if the same ESD generator is discharged, applying the same approach speed and voltage, the waveform may vary significantly.

The underlying reason is the interplay of statistical time lag and approach speed (see references for details [Pom1995, Pom1996, Chu2004]). For the cases of either a rising voltage in a fixed gap, or a closing gap at a constant voltage the time lag is defined as such: The time lag is the time between the moment the field strength in the spark gap reaches the value at which a breakdown is possible, and the moment when the breakdown actually happens.

Currently there is no industry standard method defined to obtain repeatable waveforms for air discharge. This can be technically addressed by application of a very short time lag (the time between when a discharge becomes possible and the time it occurs) to achieve the maximum arc gap distance. In the case of homogeneous fields, the maximum distance is given by Paschen's law. The values for more complex electrode arrangements is discussed in [Zho2017]. However, this approach leads to the lowest peak currents and di/dt values. Thus, the severity of the test may be significantly less compared to real world events.

As the arc length variations and the resulting waveform variations couldn't be avoided for air discharge testing in the past, in the 90's the decision was made to introduce a contact mode ESD testing procedure in IEC 61000-4-2 and to require the contact mode test whenever the discharge can occur to a conducting surface.

Within the normal variation of the arc length, which is determined by the approach speed, surface properties, voltage and humidity, there are discharges which have short arc lengths. For example, at 50% of the Paschen length the discharge current rise time can be very short (<300 ps) and can carry exceptionally high frequency spectral components and large time derivative values, leading to soft failures. Recently, it has been shown that the probability of those discharges can be reduced by using an ionizer during air discharge testing [Zhou2019]. The ionizer provides charge carriers that can initiate the breakdown once the field strength in the gap reaches a value that allows discharges to occur. An additional advantage of using an ionizer is the ability to readily discharge charged plastic surfaces. This white paper explains the initial results of a study that aims at reducing the variability of air discharge and indicates a possible path for an improved ESD test standard with reduced test result uncertainty during air discharge testing.

6.1.3 Air Discharge – ESD Generator Calibration

Many discharges that occur at the customer side are air discharges. Contact mode discharges are not recommended to plastic or glass surfaces, while air discharge may lead to sparking through gaps into metal parts, or to surface charging by corona. Thus, air discharge must be included in system level ESD testing.

Presently, there is no calibration for air discharge in the IEC 61000-4-2 standard. To address this gap, this white paper suggests a methodology to measure the step response of an ESD generator in air discharge mode. This can become a base for the calibration. It avoids the fundamental problem of all previous air discharge calibration methods as it does not involve an arc discharge [Yan2017]. Instead, it directly measures the properties of the ESD generator with high repeatability.

6.1.4 Number of Discharges per Test Point

It is well known that the ESD sensitivity of DUTs depends on the transient state of the system. This is usually caused by temporal changes in the software running on the DUT. As the time variation is not known during system level ESD testing, one cannot guarantee that the set number of pulses and pulse rate will detect the most sensitive phase. While a rigorous statistical approach is described

in [Ren1993, Wen1999, Mar2016, Rit1992, Har2016], this white paper further details test point selection, number of points and voltage levels in Chapter 8.

A relevant question could also be: Does this need to be done? If the sensitive phase is short and rare, then the likelihood of a real ESD event hitting the phase is low.

If the consequence of this ESD is not endangering safety, then the appropriate product-level cost-benefit of adding protection in such a case needs to be evaluated both by the vendor and the OEM. Such a weakness needs to be discovered before this trade-off can take place. However, the present IEC 61000-4-2 standard requires only 10 pulses per test point. Practical experience has shown that this is often not enough for achieving reliable test results. If, for example, 20 pulses per second are used, and each contact mode test point receives a few seconds of pulses, then easily 100 pulses can be applied without impacting the overall test length. This will certainly increase the likelihood of detecting sensitive phases of the DUT (note that secondary discharges must be avoided by removal of charges after each pulse as discussed in Section 6.1.11). Using such a pulse rate is common practice in many ESD test laboratories. In some cases, a test point is re-tested at 1 pulse per second if a failure was detected at 20 pulses per second. The rationale is that the DUT may not have fully recovered within 50 ms. If a failure occurs in the re-testing, also applying 100 pulses, then it is considered a failure of the test at this test point. This method seems to be a step in the right direction. For air discharge it is more difficult to apply a large number of pulses if this is performed by hand. Still, a number larger than 10 pulses per test point is needed to provide a larger coverage against software-induced sensitivity variations. Further, the arc length variation, and the consequential variation of the rise time and peak current, lead to further uncertainty in air discharge testing. Here the best method is to use automatic ESD testing with a robotic system, and to capture the discharge current at the ESD generator tip. This will identify the current waveform which caused a failure and also identify any secondary ESD. A more detailed method of selecting discharge points, voltage levels and dissipation methods is part of this white paper.

6.1.5 Transient Fields

Transient fields are not specified, and the difference in the transient fields between different brands of ESD generators is rather large: a factor of 3x at a given frequency is quite common. If a DUT has a more narrowband susceptibility, e.g., due to a resonance, then the test result may vary up to 3x by just changing the brand of ESD generator. This behavior and its root cause have been reported in [Koo2008, Koo2008b]. The present IEC 61000-4-2 standard (2008) provides information on the fields in the informative annex, but transient field calibration is not required. Further, one needs to consider that the fields of the generator depend on the orientation of the generator. Only the magnetic field within a few cm of the tip will have no angle dependence, as it is determined by the current in the tip.

6.1.6 Position of the ESD Generator

The current of the ESD generator will depend on the angle between the ESD generator and the DUT. The generator is supposed to be held perpendicular to the surface. If the ESD generator is at a different angle, the injected current will increase significantly.

6.1.7 Insufficient Contact to the Metal Part in Contact Mode

If the tip of the ESD generator in contact mode is not contacting well to the metallic surface, e.g., because of a thin paint layer, then a spark gap is created between the tip and the metal. Upon

closure of the relay in contact mode, this gap will breakdown. In most cases the rise time of the current will be much less than the 850 ps of the main discharge. This causes strong RF components and may disturb the system. Due to the uncontrolled nature of the gap this will lead to difficult to repeat results. The standard should emphasis on the importance of having good contact between the tip and the meal part.

6.1.8 Generator Calibration

Often accreditation bodies confuse calibration uncertainty with test result uncertainty. The user cares about test result uncertainty and the calibration uncertainty is often just a small contributor to the test result uncertainty. Many papers describe the calibration of ESD generators and the analysis of different influencing factors, such as the ground strap routing, the effect of the ESD current target, or the oscilloscope (+cable) bandwidth.

It is believed the contact discharge current calibration uncertainty is low, and its influence on the test result uncertainty is not strong. Therefore, to improve the repeatability of ESD test results, there is no need to improve the contact discharge current calibration. An air discharge calibration can be introduced following the method explained in [Yan2017].

6.1.9 Approach Methods for Air Discharge

The approach speed of the ESD generator in air discharge affects the development of sparks in the air discharge. The physics is well understood [Pom1995, Pom1996, Pom1998]. On average, faster approach speeds leads to shorter spark lengths, faster rise times and higher peak currents. The effect is rather strong: Reducing the spark length from 2.7 mm at 10 kilovolts (this is the Paschen value) to 2 mm at 10 kilovolts will increase the peak current time derivative from a few A/ns to > 1000 A/ns. Even if it is not possible to obtain the same rise time and peak value from each discharge, controlling the approach speed, such as is done by robotic testing, is certainly the right direction to improve test result repeatability. As mentioned above, this white paper explains initial results of the effect of using an ionizer during air discharge testing. The ionizer will help to avoid very fast rising ESD currents during air discharge testing, thus, it opens a path for reducing the test result uncertainty during air discharge testing [Zhou2019].

6.1.10 Insufficient Test Setup Specification

Presently, the IEC TC77B working group MT-12, which is responsible for of updating and maintaining the IEC 61000-4-2 standard is discussing a variety of possible changes.

6.1.10.1 ESD discharge current calibration in contact mode

Different aspects are discussed, for example, the uncertainty of the ESD current measurement and the effect of oscilloscope input reflections on the captured data. Here the Industry Council on ESD Target Levels is of the opinion that the present calibration method for contact mode is not the main reason for test result uncertainty. The calibration could be improved by testing ESD generator discharges into impedances higher than the present 2 Ohm target. The uncertainty of the captured current data is small. Any improvement of the calibration for contact mode will not help to reduce the test result variations observed by many laboratories.

Large test result uncertainties are caused by the difference in electromagnetic radiation between different brands of ESD generators. These fields are created by the voltage collapse inside the relay

which occurs in < 100 ps, while the current rise time is 850 ps. Thus, the spectral content of the current is lower than the spectral content of the voltage collapse at the relay.
So far this has been only addressed in the informative annex of the 2008 version of the IEC 61000-4-2 standard. The Council suggest that all manufacturers at least need to measure the fields around the ESD generator e.g., at a distance of 20 cm from the ESD generator at 0, 90, 180, and 270 degrees (in a plane parallel to the ground plane being discharged into) for contact mode at 5 kilovolts and publish this as specifications using a bandwidth of $\geq$ 3 GHz.

6.1.10.2 Humidity specifications

An on-going discussion topic is to narrow the range of temperature and humidity that is allowed during ESD testing. There can be various effects humidity has on ESD testing:

A) In Contact mode: The actual discharge is confined to a relay; thus, humidity does not affect the current waveform of the ESD generator. But charge decay is affected. If an ungrounded DUT is subjected to ESD, without external grounding or ionization the charge will remain on the DUT a long time. In high humidity, the charge decay times are reduced. However, this is not relevant for IEC 61000-4-2 testing, as the remaining charge must be removed before a new ESD pulse is applied as per IEC 61000-4-2 Section 7.2.4.1. A third effect relates to secondary ESD. Here, one may consider that in high humidity the statistical time lag of a secondary gap is reduced. However, most secondary gaps do not have a homogeneous E-field, as they are e.g., formed by sharp corners on PCBs. In this case the time lag is rather small. Another argument for a small-time lag is that the charge up times of secondary gaps are often very short, on the order of tens of nanoseconds. It is determined by the 330-ohm output impedance of the ESD generator (approximated) and the capacitance of the device that is not grounded, typically a few pF. Thus, a voltage much higher than the static breakdown voltage of the gap occurs. Discharges across such gaps will have very small statistical time lags.

In general, one can conclude for the contact mode: Humidity has no relevant effects in contact mode testing.

B) Air discharge: In air discharge, humidity has a drastic effect on the statistical time lag. Thus, approaching electrodes will show (on average) much higher peak currents and faster rise times in dry air. Here, one may feel a need to narrow the allowed range of humidity. Ishida [Ish2017] provided evidence. Here, air discharge testing was used to discharge between the air discharge tip and the standard current target. Both sides of the gap are rather smooth and from stainless steel. These factors lead to somewhat longer statistical time lags. The data from Ishida did not measure the spark length, but an increased spark length (probably approaching the Paschen value) is visible especially at the high absolute humidity corner of the IEC 61000-4-2 allowed specification.

6.1.10.3 Removal of the vertical coupling plane (VCP) testing

Discharges to the VCP are performed to expose a DUT to a rapidly rising electric field and to the magnetic field of the current spreading on the VCP. In addition, the DUT may be exposed to the fields from the relay structure of the ESD generator. However, the test geometry will keep the ESD generator at a distance from the DUT, such that the field exposure from the relay structure may be small.

Practical testing has shown that VCP very rarely leads to a failure that is not detected in other parts of the test. From that point of view, VCP testing may not be considered as a relevant, mandatory test.

6.1.10.4 Horizontal coupling plane (HCP) capacitance

The HCP to ground capacitance depends on:

- Distance to grounded structures, such as walls
- Size and shape
- Distance to the operator
- Equipment placed on it

It has been noted that the capacitance may vary by a factor of 1 to 2 or larger if the HCP is close to a metal wall in a shielded room (this may not be the suggested test setup, but such setups have been observed by the author many times). The capacitance of the HCP is mainly relevant after about 10 ns of a direct discharge into the HCP (in indirect ESD testing). For the first 10 ns the waves bounce on the surface of the plate and couple into the DUT. The fact that the HCP acts as a capacitor is not yet visible. Only after the reflections of the waves have ceased will the plate be considered a capacitor. It will reach a voltage that can be determined by a capacitive divider ratio from the ESD generator capacitance and the HCP-to-GND capacitance. The DUT will be exposed to a more or less static field (decay time: C_HCP * 1 megohm). Only very few DUTs are sensitive to such slow decaying fields. Keyboards, and high impedance turn on/off circuits are examples of such circuits.

6.1.10.5 Insulating layer on top of the HCP

Especially for testing of displays on mobile devices, the specification of the thickness of the insulator on top of the HCP is critical. The current standard specifies the insulator as a 0.5 mm thick plastic sheet. Two problems have been observed:

- The insulator is often not flat. Here, using a polycarbonate insulator can provide a long-term flat material
- In testing of tablets and cell phones, one test configuration is to place the display towards the HCP and to discharge to the phone. In this case, a large capacitance is formed between the DUT and the HCP. The value depends on the size of the DUT, geometry, flatness of the insulator etc. Values from 100-300 pF are typical for cell phones and tablets. Due to the discharge to the DUT all injected current will flow as displacement current through the insulator. Local variations in the flatness will lead to local variations in the displacement current density. Many soft and hard failures have been observed in the up-side down testing. A discussion is needed regarding changing to a thicker insulating layer, e.g., 5 mm. This would still lead to a large displacement current through the display, and display weaknesses could be discovered by an air discharge to the display. It would also remove the repeatability problem caused by the present test requirement.

6.1.11 Avoiding Effects of a Previous ESD Event on the Next ESD Event: Software Recovery and Charge Removal

The basic idea of the IEC 61000-4-2 testing is that each discharge is independent of any previous discharges. This has two consequences to be aware of:

1) **Software:** Any error correction or recovery triggered by the previous discharge should have completed before the next ESD pulse is applied. Now the test engineer may ask: How do I know if this is the case? There is no clear answer. For that reason, many will often apply 20 pulses/sec in contact mode and, if a failure occurs at a test point, the test may be repeated at 1 pulse/sec. Now applying 1 pulse a second for approximately 100 pulses (a large number of pulses are needed to achieve repeatability, see [Ren1993, Wen1999, Mar2016, Rit1992, Har2016]) will take time. But this is only needed at the few points at which a problem was detected.
2) **Electrostatics:** A previous ESD can charge the DUT. In this case the solution is easy, connect the DUT to ground via some high impedance path. People have used carbon fiber wire, wires with 470 kilohm resistor at each end etc. All of those will (see the exception below) not really impact the testing as they are rather invisible for RF, but they drain the charge after the ESD. The exception is secondary ESD. Consider a cell phone connected to AC power via a 2-wire charger. The 2-wire charger has no connection to ground. So, if a discharge is applied to the phone, the phone and the DC side of the charger will charge up, this may lead to a secondary ESD event inside the charger. This secondary event is known to often destroy the charger (and sometimes the phone due to over voltage from the charger). The other aspect are charges on the glass or on the plastic surface. An air discharge to an insulating surface will lead to surface charges. Although no spark is visible, current levels of up to 10 amperes can be reached as shown in Figure 34.

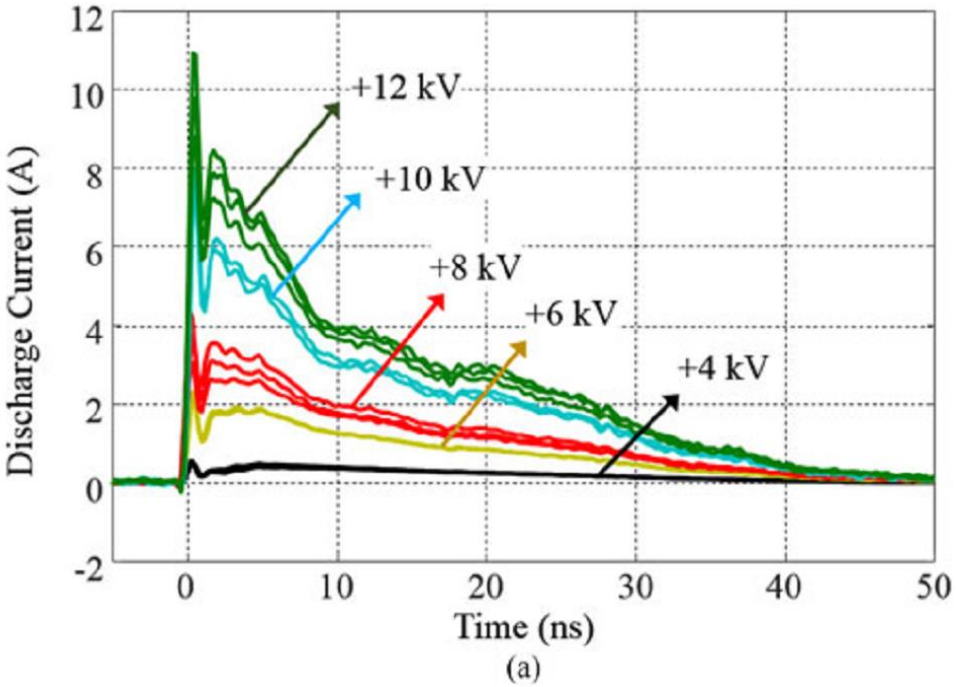


Figure 34: Discharge current for spark less discharges to a display glass [Gan2017]

The surface charge deposition can be visualized by blowing laser toner dust onto the charged surfaces. The toner powder will be attracted to the charges on the surface. The figures created this way are called Lichtenberg dust figures (see Figure 35). The method was initially published in 1776.

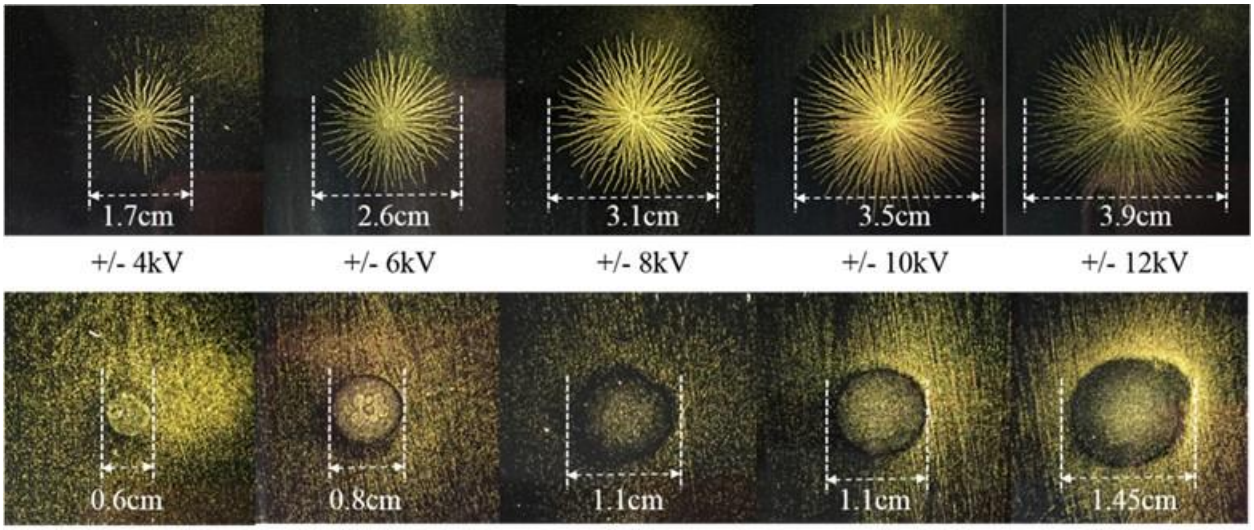


Figure 35: Lichtenberg dust figures obtained for different discharge voltage levels and polarities on a display glass surface. ESD simulator approaching speed: 0.3 m/s. Relative humidity (RH): 40% [Gan2017]. Note: top figure is positive charge voltage, bottom figure is negative charge voltage.

These charges should be removed from the glass or plastic surface. Here a brush seems to be a good method. While an ionizer will also remove the charges quickly, there is the potential risk that an ionizer will change the characteristics of the air discharge. This change can be positive for the test result repeatability. The stream of ions during air discharge testing will reduce the likelihood of very fast rising air discharge currents at higher voltages.

To allow independent testing without impact of the previous discharge the following ground rules are given:

- Use 20 pulses/sec for contact mode testing, 100 pulses at each test point and voltage level seems to be a good value (at least much better than the 10 pulses as suggested in the present standard).
- If a soft failure occurs at 20 pulses per second, retest at 1 pulse per second. If the failure does not re-occur, assume it was a result of the fast pulse rate.
- After each ESD pulse the charges must be removed to avoid secondary discharge situations.
    - For contact mode testing to parts that connect to the body of the phone a ground wire with >1 megohm is appropriate.
    - If a 2 wire AC/DC converter is used the time constant should be about 1 ms – 10 ms to GND (global GND) capacitance.
- Surface charges on glass or plastic surfaces from spark-less air discharge should be brushed off using a carbon brush or an ionizer. Note that the carbon brush should be in good shape (no worn out bristles for example) and ensure that appropriate locations be brushed (i.e. locations of ingress, floating conductors, and insulators).

6.1.12 Secondary ESD

When an ESD event reaches a non-grounded metallic part within a product, the voltage of this metal part with respect to ground will increase. If the isolation to ground is insufficient, a secondary ESD

event can occur. The discharge occurs across a spark gap between the floating and the grounded metal. The spark gap is often referred to as highly "over-voltaged." Over-voltaged means that the voltage is larger than the static air breakdown voltage of the gap. This can occur if the voltage on a spark gap rises quickly. Even if the voltage surpasses the static breakdown voltage, the breakdown may not occur due to the lack of initial electrons. This delays the initiation of the breakdown. If the voltage rise is fast, nanoseconds, the gap may reach double or triple its static breakdown voltage. Such highly over-voltaged spark gaps lead to very fast current rise once the discharge is initiated [Wan2014, Wol2015, Xia2011, Xia2012, Whi2012, Mar2017, Mar2017b, Mar2018]. The voltage across the spark gap leads to the breakdown of the spark gap and the initiation of the secondary ESD current. Secondary ESD events are especially harmful to electronic products for multiple reasons. First, the peak discharge current within the secondary spark gap can be more than five times larger than the current of the primary electrostatic discharge (ESD) event from the ESD gun [Mar2017a, Rez2017, Mar2017b, Mar2018]. Next, the rise time can be much faster than the discharge from the ESD gun. This is a consequence of discharging a highly over-voltaged gap. Third, the secondary ESD is within the product, thus, it can couple more strongly to the electronics. This can lead to soft and hard errors. From a testing point of view, another problem results from the repeatability of secondary ESD. The secondary discharge varies much more than the primary discharge due to the variability of the statistical time lag [Wan2014].

Secondary ESD is often found for:

- Non-connected metal parts in a product. These are often metal parts placed for decorative reasons
- Two wire connected AC/DC power supplies

It is important to monitor secondary ESD in a test setup. This can be done by attaching a current clamp at the tip of the ESD generator or on the ground strap of the ESD generator. The discharge currents, as captured by a current clamp can then be monitored by an oscilloscope to determine if secondary ESD occurs. If it occurs, it is essential to note this in the test report. It is suggested that monitoring for secondary ESD in ESD testing be required. It needs to be addressed when planning the experimental setup.

The secondary ESD event can be detected using software-assisted measurement techniques. The ESD gun discharge current is monitored using an F-65 current clamp at the tip of the ESD gun. The acquired current clamp waveform is further analyzed for waveform parameters such as the vertical threshold of the rising edge, the di/dt of the current waveform, and total charge delivered, which enable automatic detection of secondary ESD [Mar2018].

6.1.12.1 Timing sequence of secondary ESD

The secondary ESD event follows the primary charging event by a variable time delay (statistical time lag), ranging from nanoseconds to milliseconds. Most modern oscilloscopes offer the capability to collect separate events as a sequence of individual captures. These methods allow the scope to re-trigger very quickly (<50 ns) after an initial acquisition. The data is collected without processing to increase the re-trigger ability. Only after a sequence of trigger events is captured will the data be processed and displayed. This allows to capture sequences of pulses having a very low chance to miss a pulse. A sequential acquisition is ideal for capturing many rapidly occurring ESD events, or for capturing intermittent ESD events separated by long time gaps. The concept of

capturing a sequence of events during secondary ESD is illustrated in Figure 37. Figure 36 shows the geometry and the test setup.

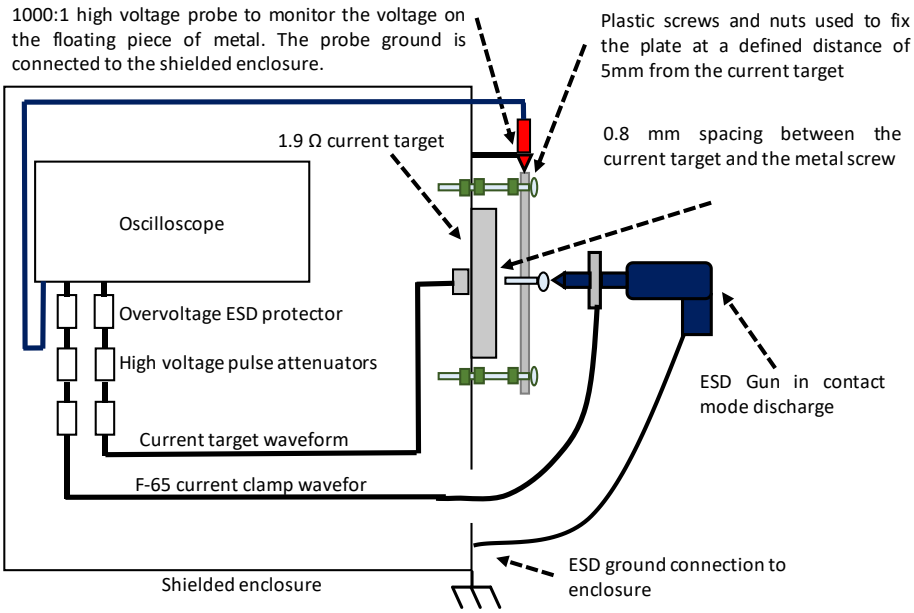


Figure 36: Geometry and test setup used for the measurement of secondary ESD of decorative metal (here a 3 mm thick Al-plate is used). The timing of the voltage charge up, primary and secondary ESD is explained in Figure 37.

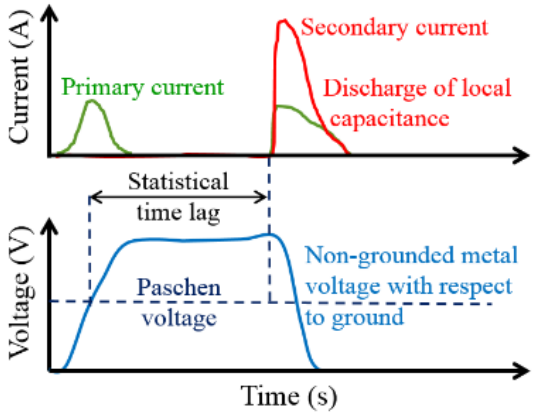


Figure 37: Graphical explanation of a typical ESD event followed by a secondary ESD waveform. The collapse of plate voltage is an indication of the occurrence of a secondary ESD event.

In general, the rise time of the secondary ESD currents is faster than that of the primary charging ESD current from the ESD gun. In real products, measuring the secondary discharge at the source location would be difficult to access and would require the use of external measurement equipment such as the wire loop antenna, F-65 current clamp, or monitoring the floating metal voltage using a high voltage probe to detect the occurrence of the secondary ESD event. In some cases, it may not be possible to access the source location of the secondary ESD event inside a real product, which will lead to a bandwidth limitation of the rise time measurements performed using the external equipment. Figure 36 illustrates a controlled setup to measure a secondary ESD event that

can be used for modeling in full-wave simulation software. The simulation model assists in predicting secondary ESD induced current levels as a suggestive guideline for worst-case rise time and peak secondary ESD discharge current.

6.1.12.2 Insufficient test documentation

Engineers are often faced with the dilemma that a product failed ESD testing. However, it is often unclear how the testing was done and reproducing the result is often impossible. Here, the variability of the test results due to software status, configuration, wire routing, ESD generator model used, etc. cannot be easily overcome. However, many test details can be documented very well using video recording (if allowed).

It is suggested that test houses record a video of the testing while the discharges are applied. This has been implemented using a foot-controlled paddle that initiates the recording of video such that it captures the ESD generator's position and approach, as much of the DUT response as possible (like screen flicker), and it starts the recording of the current by an oscilloscope. This way one can exactly associate the current and testing to an individual failure. Of course, if no failure occurs the video and current data may be disregarded.

Chapter 7: ESD Simulator Calibration Improvement

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7.0 Introduction

The IEC 61000-4-2 ESD generator calibration standard only specifies the discharge-to-ground scenario. In real measurements however, the ESD generators often discharges to different load conditions. The behaviors of the ESD generator under different load conditions are unknown to the engineers. Thus, a measurement setup which is based on an extension to the IEC 61000-4-2 standard calibration setup is proposed here to help the engineers understand the ESD generator behavior under different impedance load conditions.

Additionally, an air-discharge mode calibration method is introduced to determine the step response of ESD generators for air discharge mode.

7.1 Contact Mode Discharge into Impedances other than a Short

7.1.1 Modified ESD Target and Impedance Loads

The proposed method only slightly modifies the existing ESD generator calibration method, greatly simplifying its implementation and not requiring a different set-up. Different impedance loads are created by adding lumped components (resistor, capacitor or their combination) to the front of the ESD target. The impedance load will be referred to as the ESD target load in the later sections. The following loads are proposed (|| indicates components in parallel):

- 2 Ω (present ESD target load)
- 100 Ω
- 1 kΩ
- 10 pF || 10 kΩ (10 kΩ is needed as some ESD generator models do not discharge in contact mode without a resistive load.)
- 100 pF || 10 kΩ
- 100 pF || 100 Ω
- 100 pF || 10 Ω

These values are selected to represent the load impedance of real measurements. For example, the 100-pF load could be a discharge into a non-grounded small cell phone. The 10-pF load discharge could represent the case of discharging into a small decorative metal which may cause secondary ESD or a discharge into a car key fob. The 100 Ω, 100 pF || 100 Ω and 100 pF || 10 Ω are the values recommended by other researchers. A high resistance load investigation was reported by Nieden in [Nie2010, Nie2009], thus, a high resistance load case (1 kΩ) will be included in these measurements.

The center discharge pad of the ESD target is removed (Figure 38) and the ESD target load is then screwed into the center of the ESD target. This offers a flexible method to change the load impedance seen by the ESD generator and to measure the discharge current with high accuracy using the same set-up. A plastic tube filled with epoxy holds the resistor or the capacitor (Figure 39) to avoid high voltage breakdown and ensure mechanical stability.

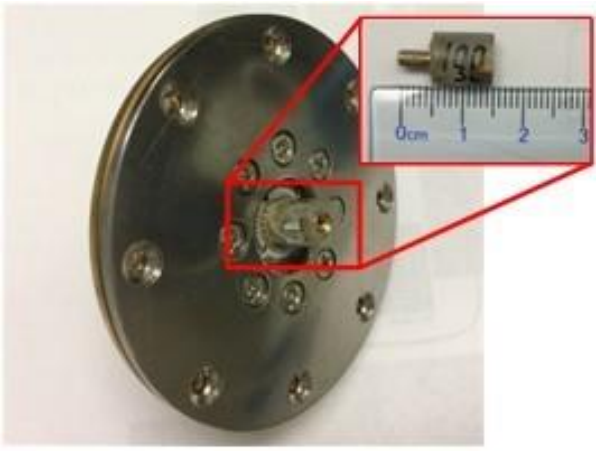

Figure 38: Load installed on an IEC 61000-4-2 ESD target. Shown is a 100 Ω resistive load

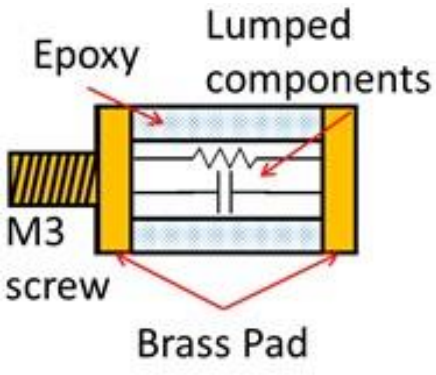

Figure 39: Structure of the ESD target load. The resistor and capacitor are embedded in epoxy.

The ESD generator discharges directly to the metal pad on the top of the ESD target load.

7.1.2 ESD Gun Calibration with a New Target Load Measurement

There are three major objectives: 1) to study the behavior of ESD generators discharging with different load impedances; 2) to offer a calibration test method for different load impedances if the experiments show that it is necessary; 3) to provide reference data for the study of the ESD generator SPICE models with different load impedances as discussed in Chapter 4.

The response to different load impedances of seven ESD generators was analyzed. These ESD generators will be referred to as “ESDGUN1 to 7” (includes 4 different commercially available models from 3 different suppliers) in the later section. Before performing the ESD target load experiments, all the ESD generators were tested using the standard IEC 61000-4-2 ESD generator calibration set-up (Figure 40, note that the use of a 20 dB attenuator may result in oscilloscope

damage for higher voltage levels, use of higher attenuation values, such as 70 dB, may be necessary). The discharge current after the first several nanoseconds is sensitive to the ground strap position. Although the strap position was as recommended for ESDGUN2, its discharge current violates the requirements (Figure 41). Because of the limited high voltage tolerance of the resistors and capacitors used in the ESD target loads, only ±1 kilovolt and ±2 kilovolts discharge levels were measured. Three discharge events were recorded at each voltage level. As shown in Figure 42 and Figure 43, the discharge current of the ESD target load shows good linearity.

If a nonlinear behavior were to be observed, the following reasons should be considered:

1) Inaccurate voltage is displayed by the generator.
2) A small voltage drop occurs across the relay after the internal spark is initiated. This drop is not a function of the current (or only a weak function) and is often in the range of 25-40 volts. For low voltage settings, the drop may lead to an observable nonlinear current increase with charge voltage.
3) Resistors may show a voltage dependent resistance value. The voltage coefficient is usually negative (resistance drops with voltage).
4) Voltage coefficient of the capacitors, especially for ceramic capacitors.

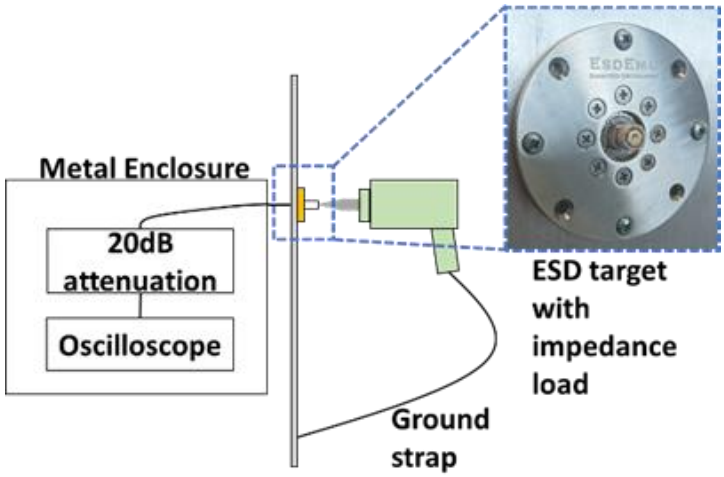

Figure 40: Measurement setup for ESD generator discharging into different load impedances, 10 GS/s, 2 GHz bandwidth. ESD target courtesy of ESDEMC Technology LLC.

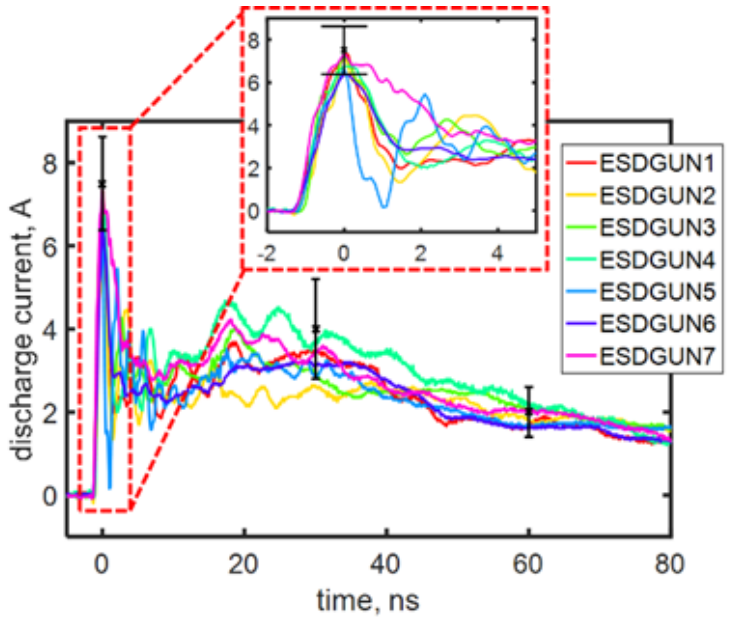

Figure 41: 2kV discharge current into a 2 Ω current target as specified by IEC 61000-4-2 (2008 release). Error bars represent the IEC 61000-4-2 limits. The error bars indicate that all but ESDGUN2 pass the requirements.

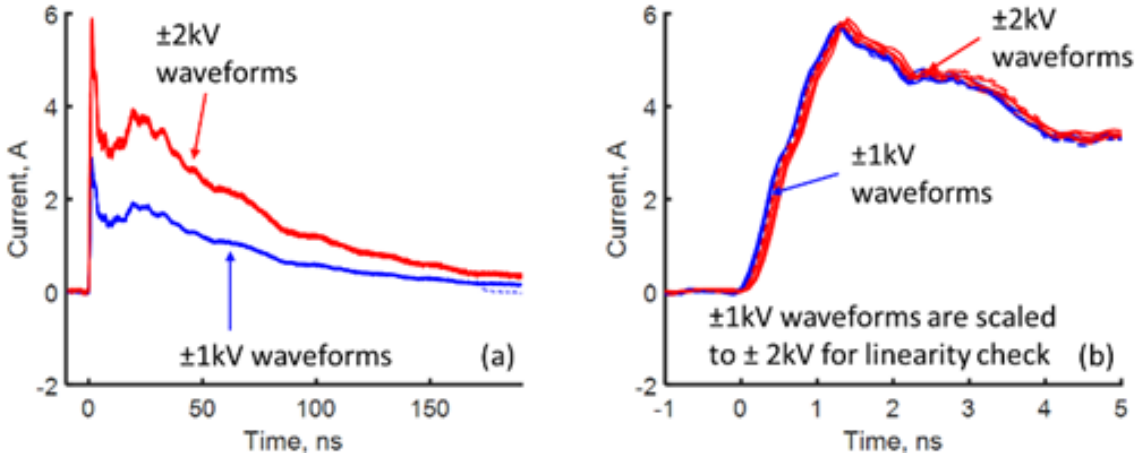

Figure 42: (a) Partially overlapping discharge current waveforms of ESDGUN7, 100 Ω load impedance. Three waveforms are shown for each discharge level. (b) Zoom-in to first peak. ±1 kV waveforms are scaled to ±2 kV; the results indicate good linearity and repeatability. Note: all negative discharge waveforms are inverted in the plot for better comparison.

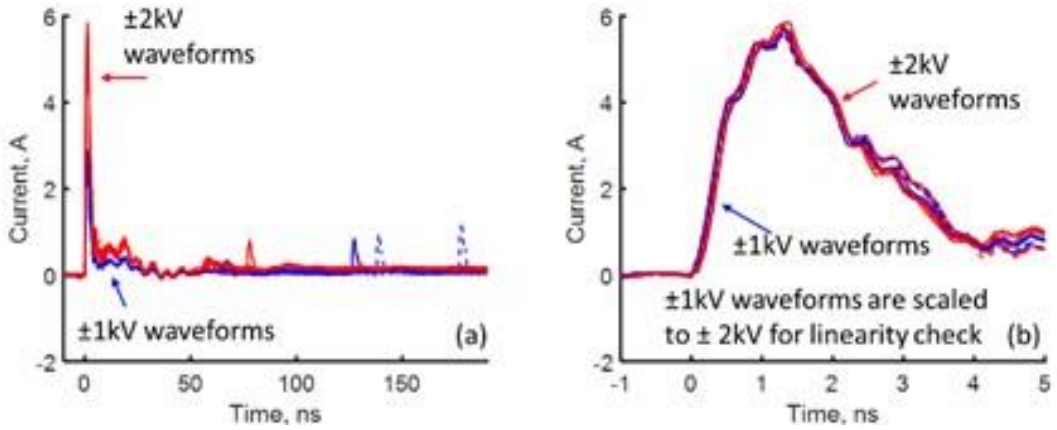

Figure 43: (a) Partially overlapping discharge current waveforms of ESDGUN7, 10 pF load impedance. Three waveforms are shown for each discharge level. (b) Zoom-in to first peak. Note: The discharge voltage levels are ±1 kV and ±2 kV. ±1 kV waveforms are scaled to ±2 kV; the results indicate good linearity and repeatability. All negative discharge waveforms are inverted in the plot for better comparison.

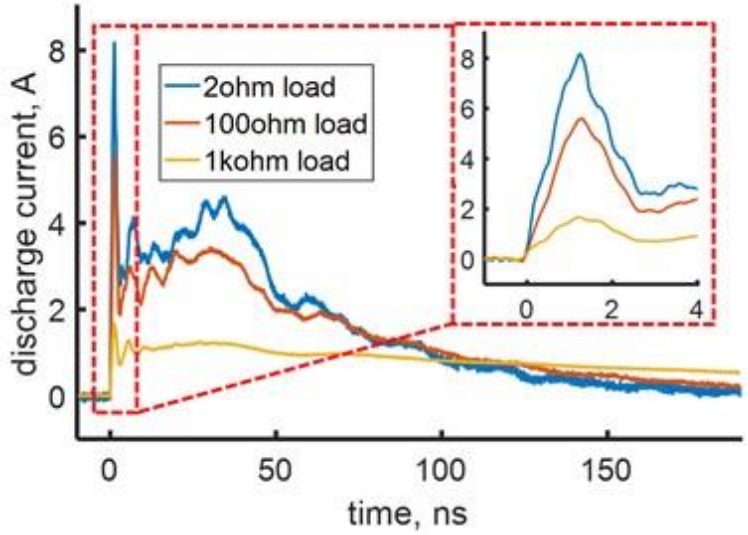

Figure 44: Discharge current waveforms for resistive loads of ESDGUN1. The discharge level is +2 kV.

To illustrate the dominating effects, the waveforms of one ESD generator are discussed in detail (Figure 44 and Figure 45). A similar behavior is observed for the other ESD generators (Figures 46 and 46). If an output impedance of a contact mode ESD generator is defined by the peak current requirement of 3.75 A/kV, a value of 266 Ω is obtained. This indicates that a generator should reduce the current from 7.5 amperes to 5.4 amperes if a 100 Ω load is used at 2 kilovolts and to 1.57 amperes if a 1 kΩ load is used. The measured average values are 5 amperes and 1.52 amperes which indicates that the simple output impedance calculation is suitable to predict the current for resistive loads. For a 10-pF capacitive load the second peak disappears while the first peak is not strongly affected (Figure 45).

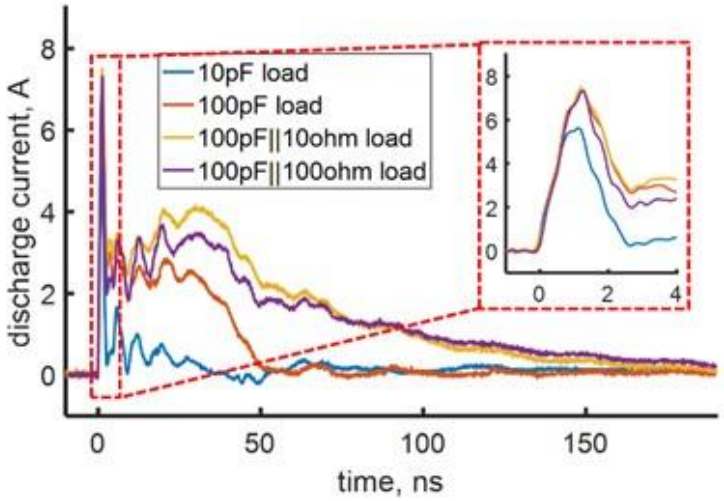

Figure 45: Discharge current waveforms for capacitive loads of ESDGUN1.

The first peak and the rise time for different ESD generators under different load impedances are summarized in Figure 46, Figure 47 and Tables 4 & 5. A load impedance of 2 Ω indicates a discharge directly into the ESD target without additional ESD target loads. Figure 46 and Figure 47 offer an easier comparison between different ESD generators. To judge if the variations between different generators at non-shorted load impedances are a concern or not, one can use the IEC 61000-4-2 peak current limits. This allows ±15% deviation from 3.75 A/kV. Figure 46 indicates that the variations for other load impedances are also within ±15% limit relative to the average values at each load impedance. Furthermore, the ESD generators show similar tendency over different load impedances; i.e., if the ESD generator has lower peak values in 2 Ω load impedance (such as ESDGUN4 vs ESDGUN7 in Figure 46), it is very likely to have lower peak values in other load impedances.

As shown in Figure 47, most ESD generators' rise times are within the range of 0.7-1.2 ns for all load impedances tested, which is within ±25% (as specified by the IEC 61000-4-2 standard for rise time variation) of the average measured values. The largest variations are observed in the high impedance load impedances (1 kΩ and 10 pF||10 kΩ). The internal structure of ESDGUN3 leads to a reduction of the rise time to only 0.3 ns rise time at a load impedance of 10 pF||10 kΩ. The average measured value of peak current and rise time for each load impedance were used as reference values in Chapter 4 which focused on ESD generator SPICE model comparison.

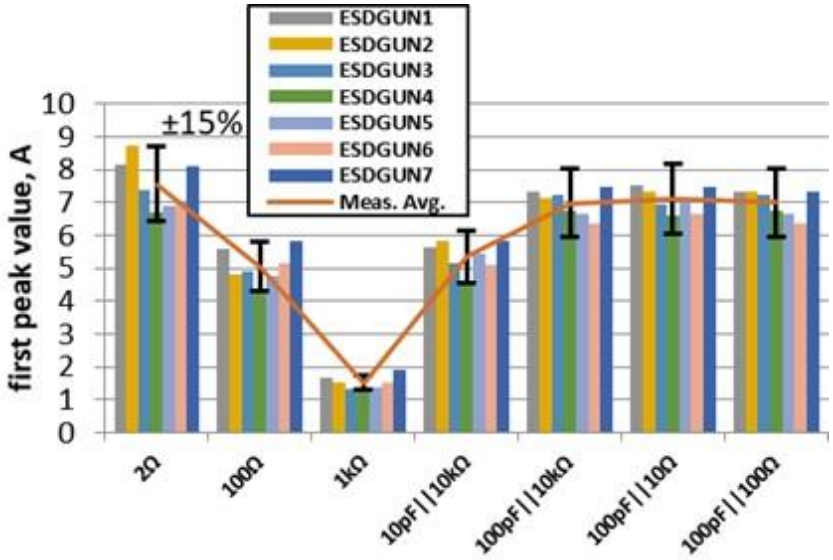

Figure 46: Value of the first peak for different load impedances. The error bars indicate ±15% variation of average measured values.

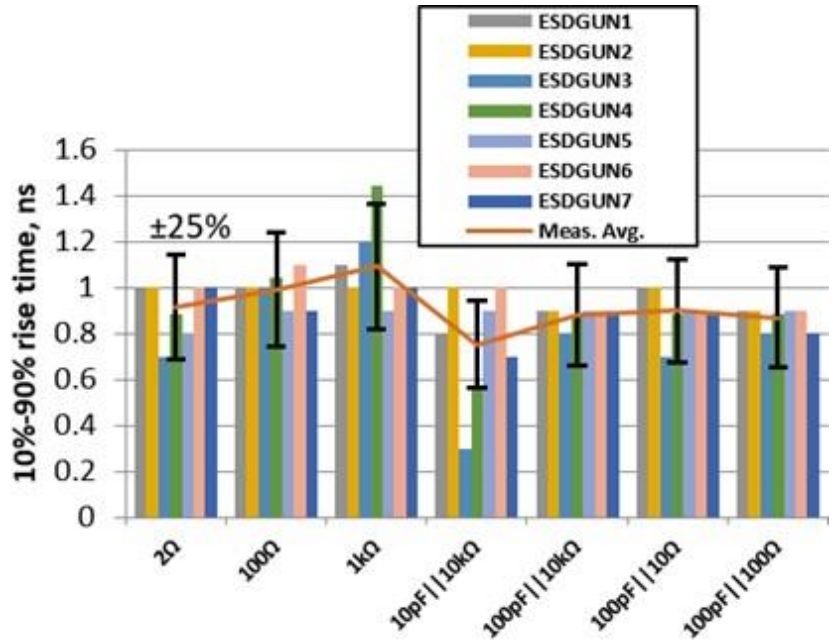

Figure 47: Rise (10%-90%) for different load impedances. The error bars indicate ±25% variation of average measured values.

Table 4: +2kV contact discharge of 7 ESD generators, first peak value. Unit: Ampere

Load impedance	ESDGUN1	ESDGUN2	ESDGUN3	ESDGUN4	ESDGUN5	ESDGUN6	ESDGUN7
2 Ω	8.18	8.74	7.39	6.72	6.92	6.99	8.11
100 Ω	5.60	4.81	4.91	4.24	4.77	5.17	5.81
1 kΩ	1.68	1.50	1.32	1.31	1.40	1.52	1.92
10 pF||10 kΩ	5.63	5.85	5.14	4.52	5.45	5.09	5.84
100 pF||10 kΩ	7.31	7.16	7.22	6.76	6.64	6.36	7.47
100 pF||10 Ω	7.51	7.35	6.95	6.60	7.15	6.64	7.47
100 pF||100 Ω	7.31	7.35	7.26	6.76	6.64	6.37	7.35

Table 5: +2kV contact discharge of 7 ESD generators, 10%-90% rise time. Unit: ns

Load impedance	ESDGUN1	ESDGUN2	ESDGUN3	ESDGUN4	ESDGUN5	ESDGUN6	ESDGUN7
2 Ω	1.0	1.0	0.7	0.9	0.8	1.0	1.0
100 Ω	1.0	1.0	1.0	1.0	0.9	1.1	0.9
1 kΩ	1.1	1.0	1.2	1.4	0.9	1.0	1.0
10 pF||10 kΩ	0.8	1.0	0.3	0.6	0.9	1.0	0.7
100 pF||10 kΩ	0.9	0.9	0.8	0.9	0.9	0.9	0.9
100 pF||10 Ω	1.0	1.0	0.7	0.9	0.9	0.9	0.9
100 pF||100 Ω	0.9	0.9	0.8	0.9	0.9	0.9	0.8

7.2 Pre- and Post-Pulses and Leakage Current Caused by ESD Generators

Besides the main current pulse, ESD generators will inject other currents into the DUT. In most cases, this is not relevant, however, if a DUT reacts to them, it can be very difficult to identify the reason. This chapter briefly treats the pre and post pulses caused by ESD generators.

The authors are aware of the following secondary currents:

- Current due to main capacitor voltage variation. Some ESD generators charge up the main capacitor and do not monitor its voltage. Now the voltage may decrease due to corona discharge. These corona currents are mainly relevant at > 10 kilovolts charge voltages. One may argue that a charged human would have the same properties: Corona may reduce the voltage. From a testing point of view one may want to have a known voltage, thus, some ESD generators have a voltage regulation circuit which keeps the voltage constant. However, this leads to another set of problems. The ESD generator may charge up a high impedance device by its recharge current.
- Leakage current. In contact mode the relay is at first open and the main capacitor is charged. However, there is a leakage current through the relay. This current, although small can charge up a high impedance device. The leakage current strongly depends on the charge

voltage, and the age of the relay. It is time dependent, initially, after charging the capacitor it may reach 1uA.

- Pre-pulses. Depending on the circuit of the ESD generator (e.g., usage of one or two relays) pre pulses can occur from the charge up process of the capacitor.
- Post pulses. After the initial pulse, additional pulses can occur due to re-ignition of the arc, and due to charge up of the main capacitor.

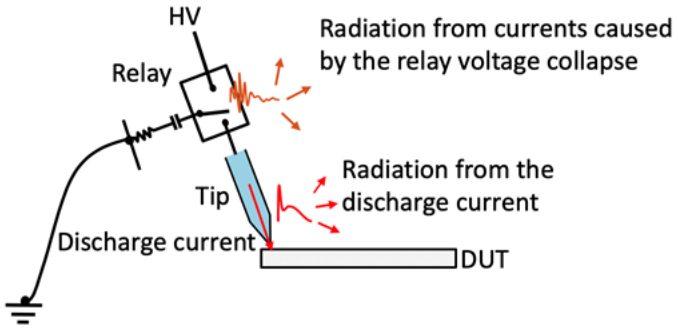

Figure 48: Illustration of the radiation sources during ESD testing

The radiation from the discharge current (see Figure 48) has been well studied [Koo2008] to correlate the failure level with the characteristics of the discharge current, e.g. the rise time, the maximum current derivative or the spectrum. However, the radiation from the currents caused by the relay voltage collapse is an often-neglected factor during ESD testing.

7.2.1 Multiple Pulses in Air Discharge

In an air discharge, the main pulse may not completely discharge the main capacitance of the ESD generator. The spark may quench leaving a residual charge in the main capacitor. Upon further approach, subsequent discharges occur which will deplete the remaining charge in the main capacitor. These secondary ESD pulses have lower peak amplitude, but much faster rise time. Here it needs to be considered that a human-metal (H-M) pulse in air discharge from a discharging person may also have the same features. The total transferred charge (transferred in multiple pulses) will not surpass the total charge stored in the main capacitor and local stray capacitance of the ESD generator.

The second situation, which may cause pulses, has been observed on ESD generators which have a cable connection to a high voltage supply. The capacitance of the cable and possible capacitances inside the base unit will recharge the main capacitance of the ESD generator. The speed of the recharge depends on the charging resistor value and having a second relay in the hand-held unit will prevent this type of recharge. However, if it occurs, it can lead to subsequent ESD pulses after the main pulse, finally (sum of the charge of all pulses) surpassing the charge value stored in the main capacitance, as additional capacitances (e.g., cable capacitance) are discharged.

7.2.2 Pre/Post Pulses

Pre/post pulses, also seen in the transient fields if the tip is not connected to anything, are usually caused by the charge-up phase of the ESD generator. The ESD generator may close a relay, which suddenly charges structures inside the ESD generator. This rapid charging can cause transient field

pulses having rise times < 300 ps. A similar charging process can also occur when the relay moves back to the charging position depending on the structure of the generators.

Figure 49 shows an ESD generator model including the parasitic parameters. When the relay closes on the A side to charge the main capacitance C_1 the local ground will move in potential, and contact A will drop in potential. This will lead to a current injection at the tip via C_{p4} and C_{p7}.

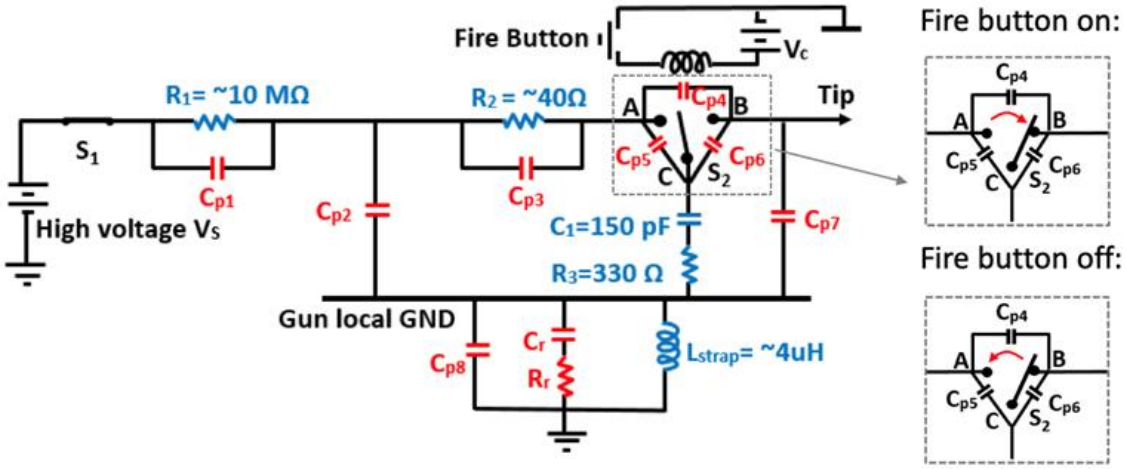

Figure 49: ESD generator model including some parasitic parameters

As the ESD-induced soft failure is mainly caused by the disturbance of the field, the induced voltage measured by a 0.5 cm^2 loop probe is used as an indicator for the transient magnetic field. Two types of post pulses were observed. The time sequence of such an example is shown in Figure 50.

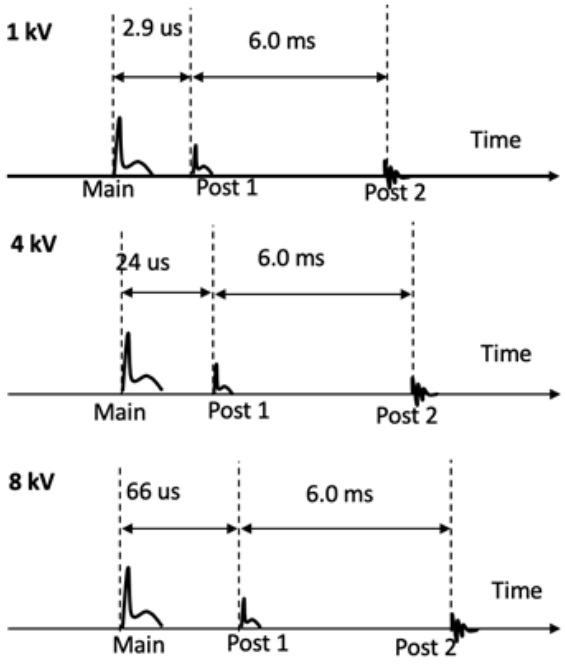

Figure 50: Time sequence of the pulses during an ESD discharge

The first post pulse is caused by the relay re-ignition of the spark within the relay. This is identified by the fact that the current waveform has similar waveform shape with the main pulse, and the time difference depends on the voltage. The second post pulse is caused by the relay. The 6.0 ms delay represents the relay mechanical movement. The timing is not affected by the charge voltage. The pulse is caused by the charge up of the structure, with emphasis on the high frequency components. The waveform at 8 kilovolts is shown in Figure 51.

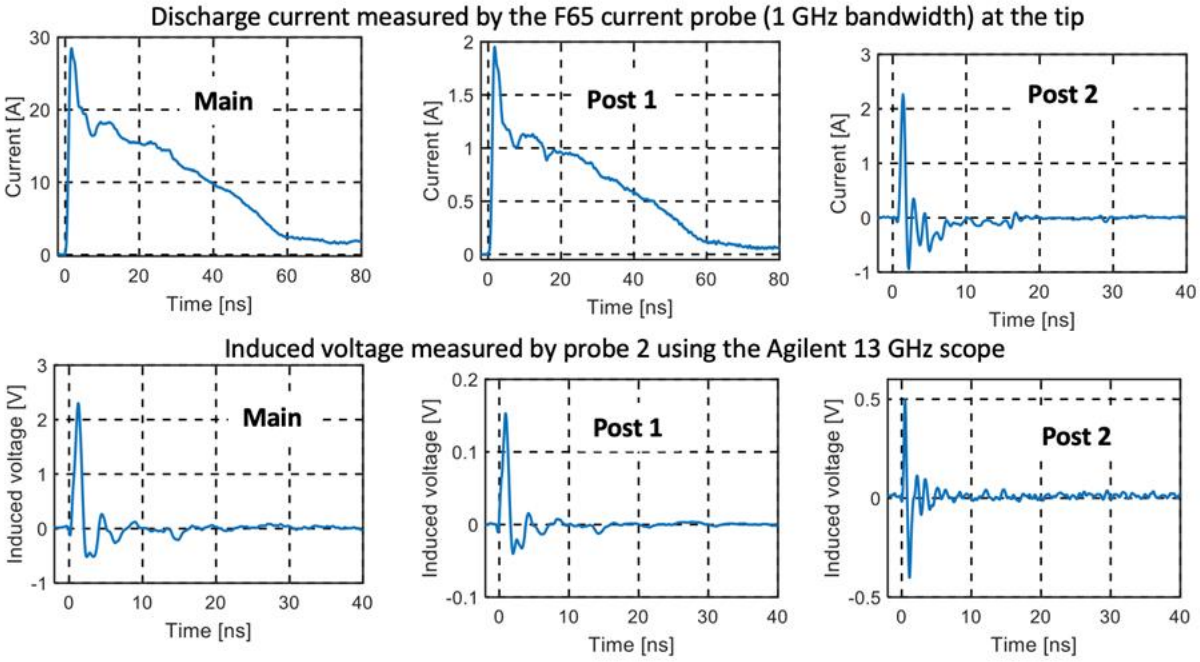

Figure 51: Discharge currents measured at the gun tip and the induced voltage measure by a 0.5 cm^2 loop probe at 8 kV. The probe is placed at 20 cm, oriented to capture the main field component.

As Wang etc. [Wan2004] has shown that the devices subjected to the ESD-induced fields can be sensitive to a certain range of the spectrum, it would be challenging to reproduce the test results when the post pulse is stronger than the main pulse for certain generators. An example is given for a generator that has been tested when the loop-measured induced voltage is 10 dB higher for the post pulse than the main pulse in the frequency range from 2.4 GHz to 2.8 GHz, see Figure 52.

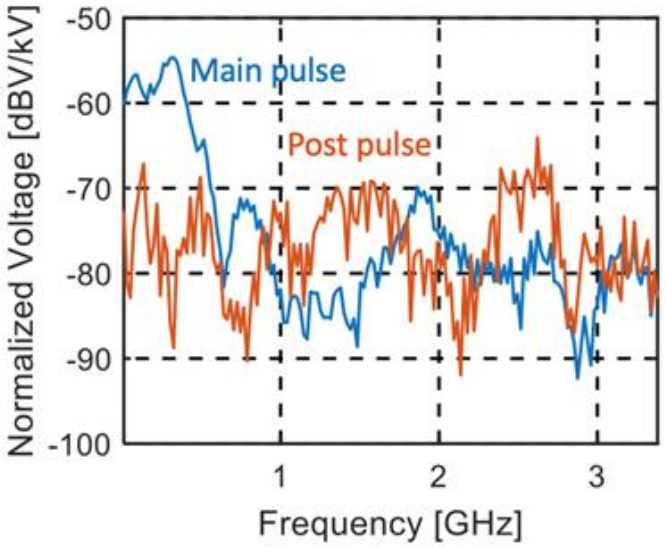

Figure 52: Comparing the spectrum for the main pulse and post pulse at 8 kV.

The Industry Council on ESD target levels suggests adding guidance to the IEC 61000-4-2 standard which:

- Informs the user and ESD generator manufacturer about pre and post pulses
- Ask manufacturers to quantify the leakage currents
- Ensures that these pre and post pulses are significantly weaker than the main pulse, both for current and fields.

7.3 Improved Air Discharge Calibration

Many electronic products must comply with IEC 61000-4-2 [IEC2001] and/or ISO [ISO2001] ESD immunity standards before entering the market. Contact discharge and air discharge are considered in these standards and have been analyzed in [She2014, She2015 and Zho2016]. In the contact discharge measurement, the ESD generator (also known as "ESD gun") tip contacts directly with the DUT. The discharge occurs when the internal relay of ESD generator closes. In the air discharge measurement, the internal relay is kept closed as the charged ESD generator approaches the DUT. The discharge in the air gap between the ESD generator tip and DUT can occur when the distance reaches a certain length. The current carrying charge carriers within the spark can either originate from surface processes or a result of gas discharge processes [Sve2002].

For contact discharge, the discharge current waveforms are highly repeatable because the high voltage spark only occurs inside the ESD generator's internal relay, which is filled with inert gases such as SF-6 and N_2. Thus, it is possible to specify a standard waveform for a contact discharge measurement. On the other hand, for an air discharge measurement, it is well known that the current waveforms have poor repeatability due to the variations of the spark resistance which results from the variation of the spark length. The variations of the arc length are a result of the approach speed and the statistical time lag. The statistical time lag is affected by humidity, surface conditions, voltage, etc. [Pom1993]. Thus, it is difficult to define a reference current waveform for air discharge calibration.

To produce better repeatability in the discharge current in an air discharge mode, two approaches exist:

1) Discharge at a spark length given by the Paschen equation [Pom1993, Rit2015, Zho2017, Yua2010 and Bor2008]. This can be realized by slowly approaching the ESD generator, possibly combined with methods that reduce the statistical time lag. Here, strong ultraviolet (UV) light, high humidity, and graphite layers on the electrodes can be used. If this method is selected, the discharge waveforms will repeat well, especially above 5 kilovolts. However, the current rise time will be rather slow (e.g., 3 ns at 10 kilovolts) as the long arc length leads to a slow drop in the arc resistance. The rate of change of the current for voltages above 3 kilovolts will be in the range of a few A/ns. Thus, the arc is stabilized at a low threat level. The step response of the ESD generator and high-frequency components of the current waveform and fields will be suppressed by the slow drop of the arc resistance. Thus, the test is more about determining the selection of the main RC components of the ESD generator. In addition, Ishida et al. proposed an air discharge calibration method based on a fixed gap discharge [Ish2016]. The idea is to use a fixed gap to replace the varying distance between ESD gun tip and the ESD target of the typical air discharge measurement. The process used spark gaps from Paschen length, down to 1/3 of Paschen length. The shorter, strongly over-voltage gaps lead to fast rise times and high peak currents. As the spark length is fixed, the waveforms are repeatable. However, they are still influenced by the time varying spark resistance. Another condition for this method to work is that the voltage rise, which is initiated by closing the internal relay is much faster than the statistical time lag. Otherwise, it is possible that the discharge may already occur while the voltage is rising.

2) If a low voltage is used and the ESD generator approaches the ESD target quickly, the arc resistance may approach an ideal step function. One would hope that its resistance changes from infinite to nearly zero in picoseconds. Achieving this would allow capturing the step response of the ESD generator. The problem is that the spark gap formed between the ESD target and the ESD generator tip does not act as an ideal switch even at fast approach speeds. The method suggested in this white paper (see Section 7.4) improves this concept by using a Mercury wetted relay that approaches an ideal switch much better.

The calibration approach presented in this white paper avoids testing ESD generators in actual air discharge mode that have a spark at the tip. The proposed method measures the step response of the ESD generator in air discharge mode using a Mercury-wetted relay. The details of the structure and measurement set-up are explained in Section 7.4. Human body discharge step response was also measured using the same Mercury relay set-up. The measured human body discharge waveform can serve as a reference for the air discharge mode waveform for air discharge calibration.

7.4 Step Response Method for Air Discharge Calibration

7.4.1 Step Response Method using Mercury-wetted Relay

To measure a good approximation of the step response of the ESD generator a Mercury-wetted relay is mounted between the tip and the ESD current target. The additional structure has a length of 16.4 mm. It substitutes the actual spark (Figure 53). ESD current targets have a discharge pad at their center [IEC2001]. In this measurement, the discharge pad is replaced with the Mercury relay

which is enclosed into an epoxy filled tube to ensure mechanical stability. The relay is activated once a permanent magnet is brought into its proximity.

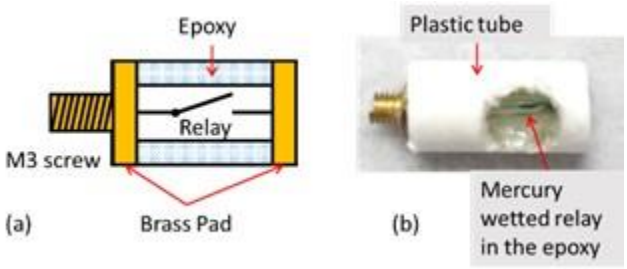

Figure 53: The diagram (a) and photo (b) of the Mercury relay tube

7.4.2 Step Response Measurement for the ESD Gun

The Mercury relay tube is screwed onto the center of the ESD target (Figure 54). The selected relay cannot withstand voltage higher than 2 kilovolts, so measurements were performed at 1 kilovolt. An Agilent DSO81304A oscilloscope was used in the measurement (40 GS/s, 12 GHz bandwidth). Three ESD generators from different manufacturers were tested. They will be labeled as "ESDGUN1", "ESDGUN2" and "ESDGUN3" in the measurement results section.

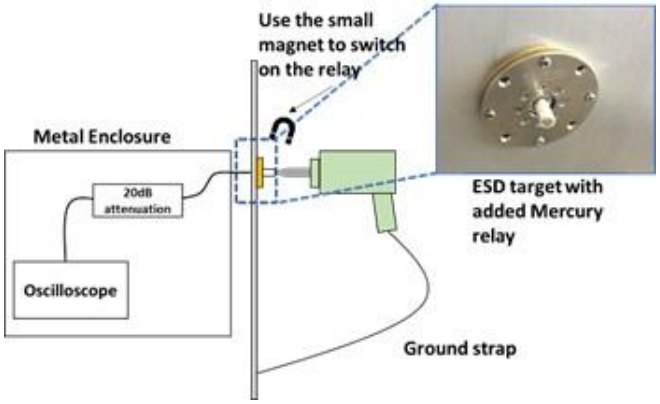

Figure 54: Mercury wetted relay attachment screwed into the center conductor of the ESD current target.

7.4.3 Step Response Measurement for the Human-metal Discharge

The event of a human discharging via a hand-held metal forms the reference event for the IEC 61000-4-2 standard, and it can be tested as to how similar the step response of the air discharge mode generators is to the human-metal discharge event. As shown in Figure 55, the person is standing on a piece of Styrofoam for insulation. A high voltage supply ensures the correct charge level. The tester holds the air discharge tip against the Mercury relay when the step response is measured. The discharge current and transient field of two testers were measured, the text refers to them as "Person1" and "Person2".

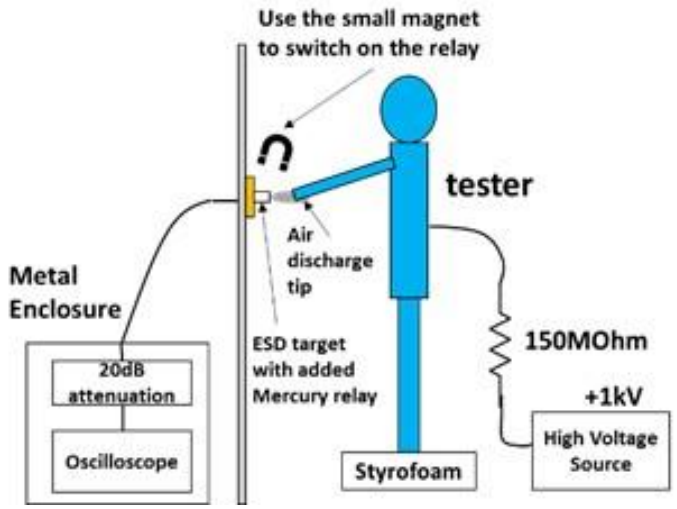

Figure 55: Illustration of human-metal discharge step response measurement.

7.4.4 Transient Field Measurement

Previous research has shown that the transient field of ESD generators in contact mode differ strongly, especially in the higher frequency region [Koo2008]. The variation in the transient field often causes different equipment under test (EUT) failure levels when using different ESD generators. Thus, it is necessary to investigate the transient fields of the ESD generator in air discharge mode. Following the methodology outlined above, the transient fields during a step response excitation were captured. Figure 56 shows the set-up of the transient field measurement. A shielded loop probe having a loop diameter of 1 cm is used for H-field measurement. The E-field sensor which was shown in [Chu2004] is used in the measurement. The E-field sensor has a flat response from 2 MHz to 2 GHz. On the other hand, waveform deconvolution [Yan2017] is needed for the H-field data as the sensitivity of the loop probe drops at lower frequencies by 20 dB/dec. The H-field probe is good up to 2 GHz. The transient fields at a 10 cm and 40 cm distance from the ESD target center were measured. The discharge current, E-field, and H-field of the same discharge event can be recorded simultaneously. It should be noted that the transient field of the ESD generator discharge event is NOT rotationally symmetric [Koo2008]. The E/H fields in this set-up were measured at different locations (Figure 56).

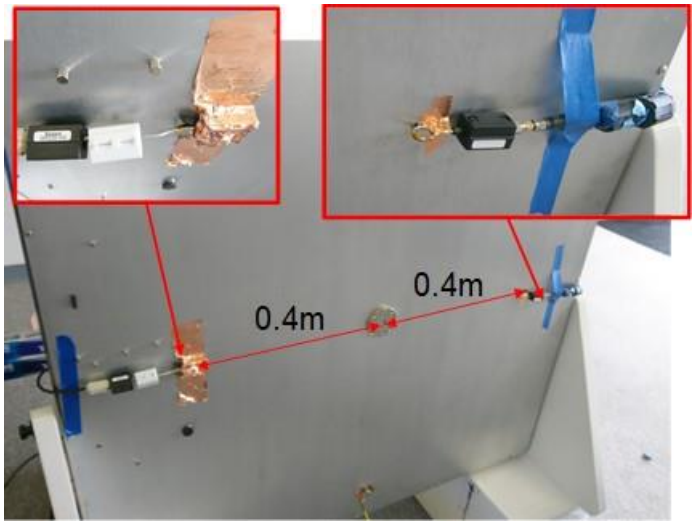

Figure 56: E- and H-field measurement set-up, based on the IEC 61000-4-2 ESD generator calibration standard. The frequency response of the E-field probe is flat from about 2 MHz to 2 GHz. The frequency response of the H-field probe has been deconvolved mathematically.

7.4.5 Repeatability

Achieving repeatability is the main challenge for every air discharge calibration method. The Mercury-wetted relay is the best possible approximation of an ideal switch. Thus, this relay has achieved excellent repeatability in both human metal and ESD generator discharges.

7.4.6 Discharge Current

The data shown in Figure 57 compares ESD generators and discharges from people holding the air discharge tip in their hand. The step response and the initial rise of each waveform is similar. The rise time is determined by the "ideal switch" formed by the Mercury relay, and it is also limited by the bandwidth of the oscilloscope. Since the ESD target shows ideal impedance up to 5 GHz, the measured discharge current data will be filtered by a 5 GHz first-order low pass filter. The discharge current of ESDGUN1 in contact discharge mode (black dotted line) is also shown in Figure 57.

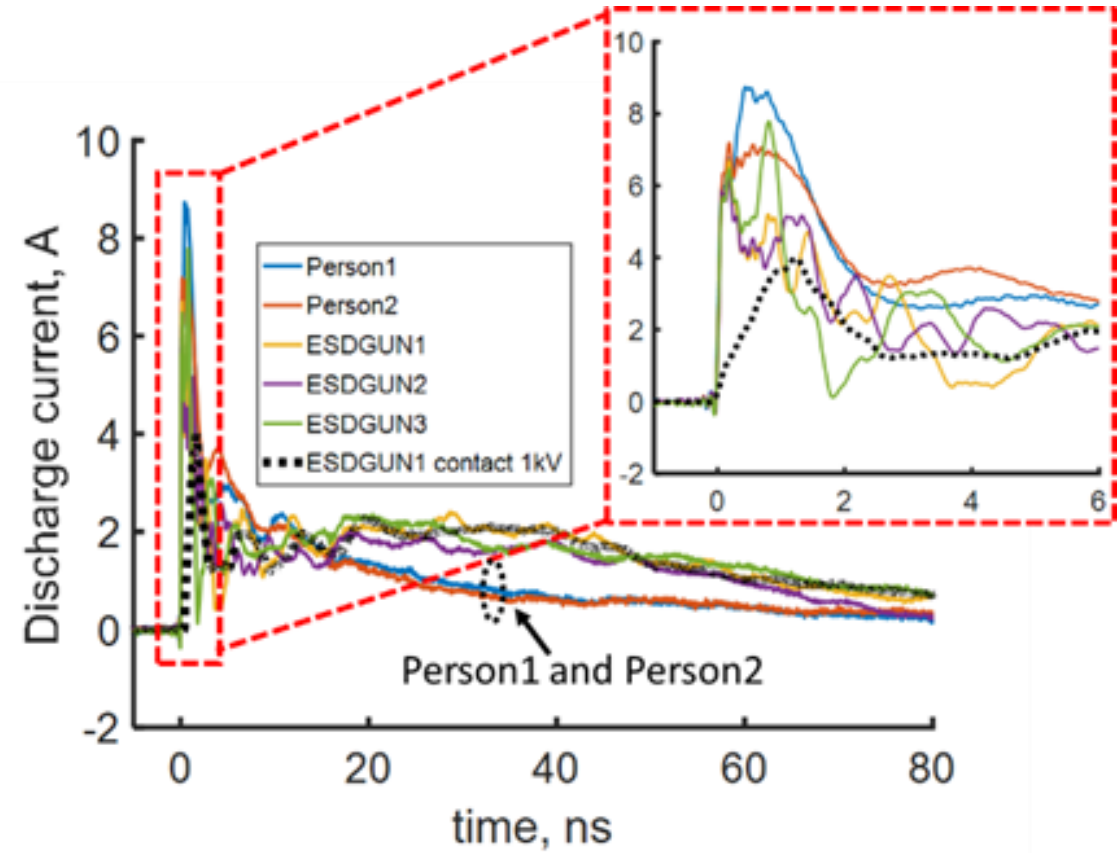

Figure 57: Step response currents for three ESD generators and two people.

Core findings from the discharge current comparison in Figure 57 are:

1) The measurement method gives repeatable step response information that allows characterization of the ESD generators in air discharge mode without having any effect of an arc (repeatability not shown in the Figure 57).
2) The peak values of these three generators varied between 6.4 amperes and 7.8 amperes, which are well within ±15 % of the average measured ESD generator peak values for a charge voltage of 1 kilovolt (a larger sample size of ESD generators may show higher variations between ESD generators).
3) Comparing the 1 kilovolt ESDGUN1 air discharge step response (yellow solid line) to the contact mode discharge (black dotted line) reveals a 2.6 amperes larger peak current value which is partially explained by the difference in rise time. There is also significantly more charge in the initial peak of the step response due the charge on the stainless steel tip. The later parts of waveforms (after 10 ns) almost overlap. This results from having the same RC network for contact mode and the step response.
4) The human metal ESD event ("Person1" and "Person2") showed larger current values of 7 amperes to 8.2 amperes. This is caused by the local capacitance of the hand that is close to the grounded wall. This structure is bulkier than the tip region of most ESD generators leading to a higher current in the step response (Figure 55). The total charge of the human metal ESD was less than the total charge of the ESD generators. This is to be expected as in most cases the capacitance of a human to ground is less than the 150 pF as specified in the IEC 61000-4-2 standard. Human to ground capacitance can be as low as 70 pF in a wood frame house

[Tal2016], but the capacitance can be double that standing (insulated) on a conductive floor. For that reason a person charged with the same amount of tribo generated charge can have twice the voltage in a wood frame house as they would have on a conductive floor.

5) All air discharge ESD generators showed ringing in a different frequency. The human metal ESD does not show the double peak structure which is (for historical reasons) part of the IEC 61000-4-2 standard's reference waveform.
6) It is known and has been reported many times that the human metal ESD only rarely shows the clear double peak structure [Pom1996].

7.4.7 Transient Field Results

As the current flows through the ESD generator, the transient field must be part of the discharge. However, there are fields that are caused by the relay. Thus, a real human-metal ESD would not have such fields. On the other hand, a human metal ESD may have much faster rise times, thus causing strong EM fields. The setup of the field measurement is shown in Figure 56.

The following conclusions can be drawn from the electric field results in Figure 58 at a 10 cm distance:

1) The peak field strength at 10 cm is between 4.5 and 5.5 kV/m at a 1 kilovolt charge voltage. In a real air discharge situation, it is not expected that the field strength increases linearly with voltage, as the rise time would typically increase with voltage.
2) The human metal ESD event shows a much larger electric field in the later time of the waveform as a result of having a charged body. In contrast the ESD generators store the energy in a discrete capacitor. Thus, these fields are not visible outside the ESD generator.
3) The rise time is determined by the relay and the field sensors' bandwidth (about 2 GHz); thus, it cannot be attributed to properties of the ESD generator.

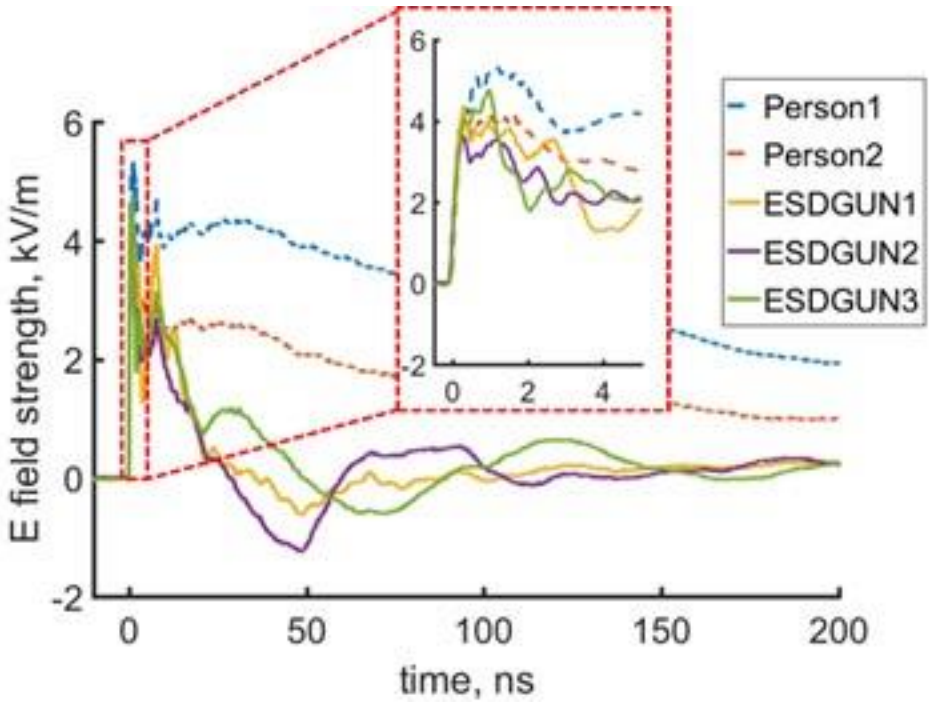

Figure 58: E-field of the step response measurement result at 10 cm at +1 kV for three ESD generators and two human metal discharges, the measurement bandwidth is limited to 2 GHz (E field sensor) at a 1 kV charge voltage. Discharge is performed via Hg relay.

The magnetic field data in Figure 59 shows that

1) The peak values are in the range of 9 A/m-11 A/m for the cases investigated at 1 kilovolt.
2) The rising edge is determined by the Mercury relay, not by the ESD generators.
3) The H-field waveform shapes are similar to the corresponding discharge current waveforms at this distance.

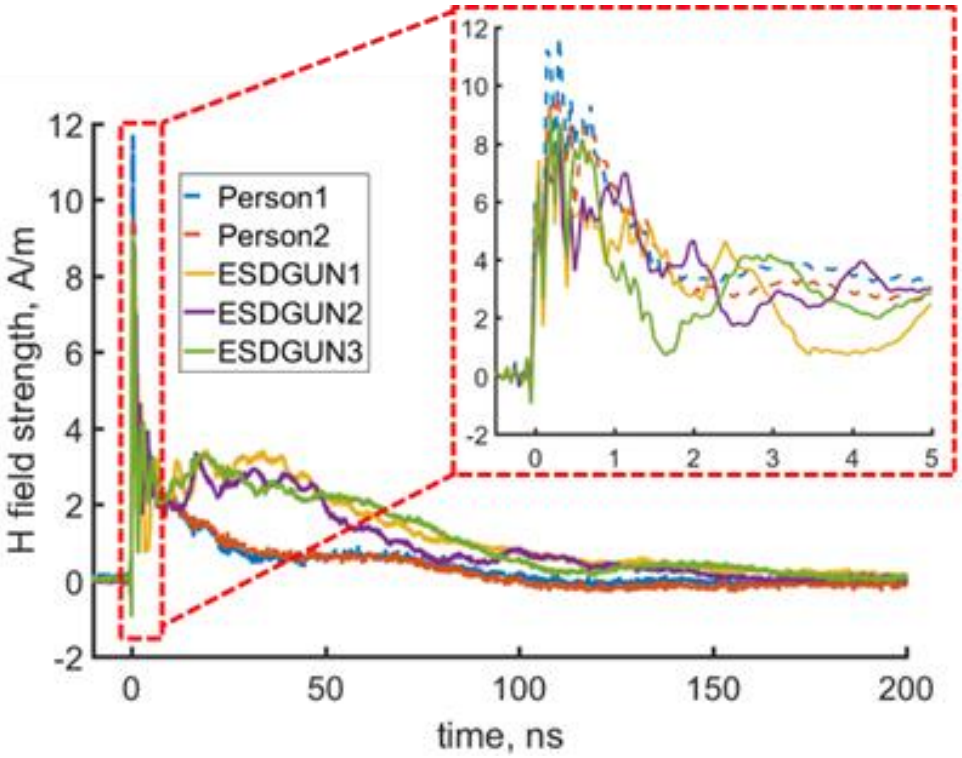

Figure 59: Deconvoluted H-field of the current step response measurement at 10 cm at 1 kV for three ESD generators and two human metal discharges. Discharge is performed via Hg relay.

The E-field sensor and H-field sensor were placed 40 cm away from the ESD target center. The setup of the field measurement is shown in Figure 56. The discharge current, E-field and H-field waveforms were recorded at the same time by the oscilloscope as shown in Figures 60 and 61.

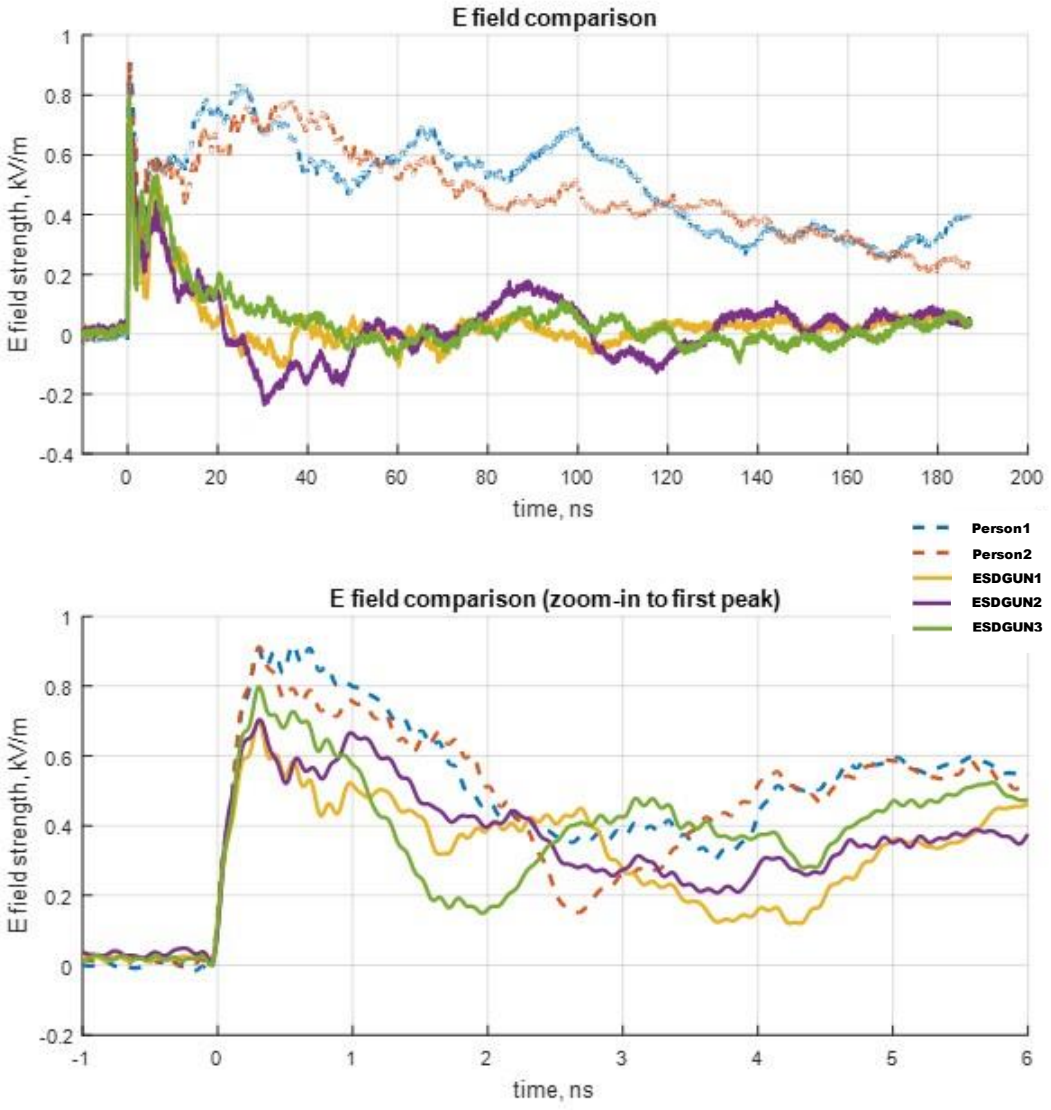

Figure 60: E-field measurement result at 40 cm at 1 kV for three ESD generators and two human metal discharges, the measurement bandwidth is limited to 2 GHz. Gun are discharged in contact mode. Persons discharged via air.

The following conclusions can be drawn:

- The field strength at 1 kilovolt and 40 cm is between 0.7 – 1 kV/m. In a real air discharge situation one could not expect that the field strength increases linearly, as the rise time would increase with voltage.
- The human metal ESD shows a much larger electric field in the later time of the discharge. This is a result of having a charged body. The ESD generator stores the energy of the charged body in a discrete capacitor, thus, these fields are not visible outside the ESD generator.
- The rising edge is determined by the relay and the scope bandwidth, thus, it has no relationship to the ESD generator.

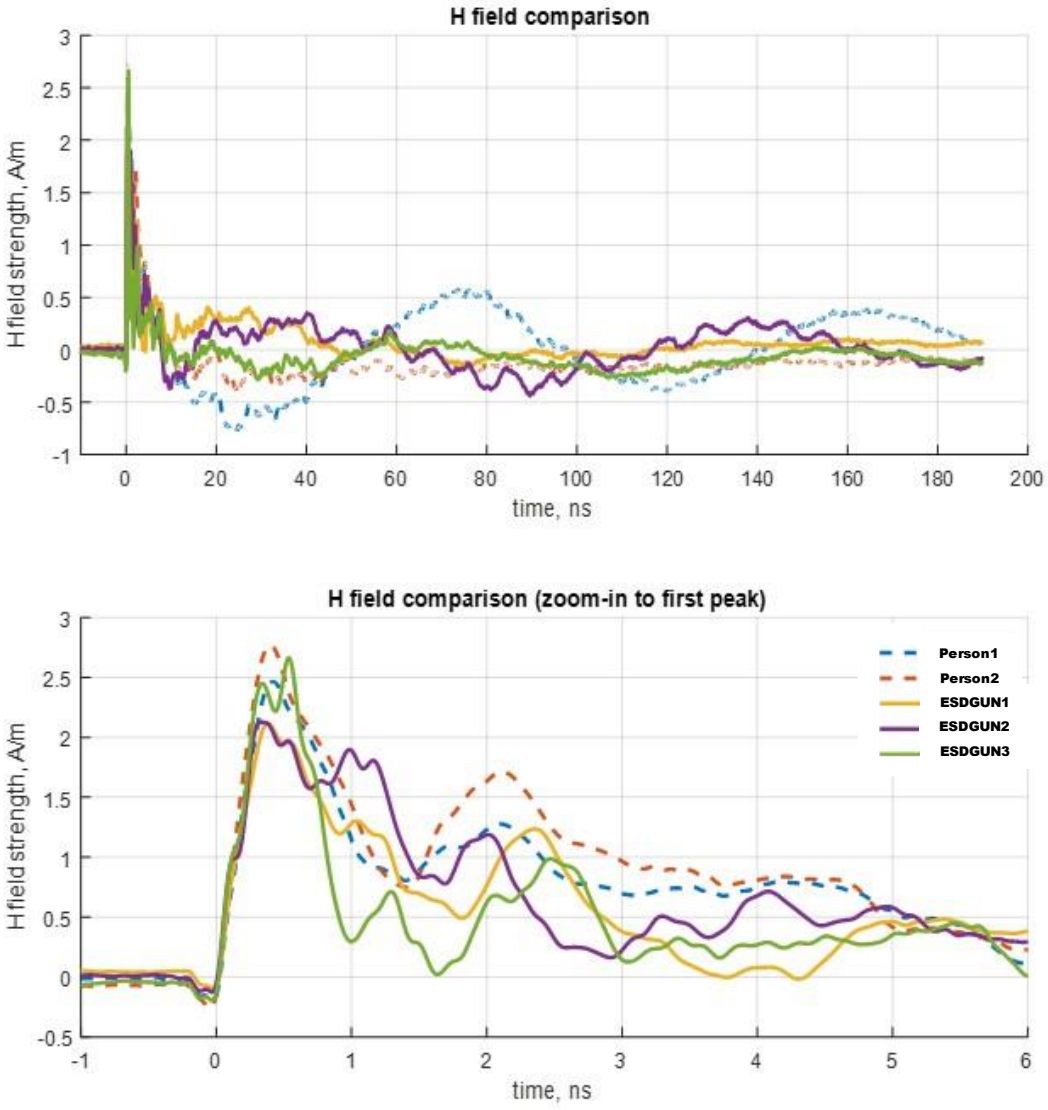

Figure 61: H-field measurement result at 40 cm at 1 kV for three ESD generators and two human metal discharges. Gun are discharged in contact mode. Persons discharged via air.

The magnetic field data shows:

- The peak values are in the range 2.1 A/m – 2.8 A/m for the cases investigated at 1 kilovolt
- The rising edge is determined by the mercury relay, not by the ESD generators
- All ESD generators and the human show ringing, the belief is that some of the ringing may be caused by the test setup (e.g., the 90 ns ringing seen in every waveform).

The Mercury relay measurements are highly repeatable. Thus, this method has the potential to be a calibration method of an ESD generator in air discharge mode.

7.4.8 Discussion

The air discharge is well known for its poor repeatability due to the variation of the spark length for approaching electrodes. Several attempts have been made in the hope of defining a calibration method for ESD generators in air discharge mode. Greatly improved repeatability can be achieved either by a fixed gap [Ish2016] or by only considering discharges at spark lengths defined by Paschen's law. Although carefully controlling the experimental parameters such as approaching speed, humidity, and air pressure can improve repeatability, it is not possible to achieve the repeatability of contact mode if a spark is part of the testing. The proposed method overcomes this by avoiding the arc and capturing the step response of the linear ESD generator. The measured currents and fields are well repeatable in using the Hg relay, repeatable enough that differences between different brands of ESD generators become clearly visible. The data also indicates that the peak current variation between different brands of ESD generators (sample size of only three) is in the same range (within ±15%) as accepted for contact mode. As the spark is substituted by a relay, no useful rise time measurement can be performed. This is not considered as a disadvantage, as the rise time in air discharge is determined by the drop of the arc resistance, and the arc physics is independent of the specific model of ESD generator used. Another possible limitation which was not investigated further is the nonlinear effects, such as the usage of a ferrite in the ESD generator which may lead to nonlinear effects at higher charge voltages. However, as the same ferrite would be used in contact mode, such nonlinear effects could be captured during the contact mode calibration. Overall, the proposed method combines the advantages of only modifying the test setup slightly, with directly measuring the step response, such that it may enable creation of a practical air discharge calibration method.

7.4.9 Conclusion

A calibration method is proposed in this section for an ESD generator air discharge measurement. The method is based on the step response which is realized by using a Mercury-wetted relay. The experiment has shown very good repeatability for discharge current and field measurement. The Mercury relay measurements are highly repeatable, and it excludes any arc effects. Thus, the data shows the effect of design choices within the ESD generator contact mode specification. This method has the potential to be a calibration method of an ESD generator in air discharge mode.

Chapter 8: Improved Test Practices

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Dr. David Pommerenke, Graz University of Technology

The IEC 61000-4-2 standard is a compliance test: it describes the minimum ESD immunity many consumer electronics products must pass to comply with legal requirements for sale in a country. However, the IEC 61000-4-2 standard says nothing about the field reliability of products that pass this compliance test: the test cannot predict the ESD reliability of the products in the hands of customers! Companies that make and sell consumer electronics products need to predict the field reliability of their products, to satisfy customer expectations, meet warranty requirements, and preserve company brand reputations. This chapter explains a new technique to test products and analyze the test results that enables accurate prediction of the ESD reliability of these products in the hands of customers. This new technique is not intended to replace the IEC 61000-4-2 standard but may prove useful guidance for future updates of IEC 61000-4-2.

8.0 Voltage Levels

People commonly associate ESD with charges accumulated by walking on carpet and touching a doorknob. However, it has been shown that the voltage levels acquired from walking on carpet are often much lower than voltages obtained from:

- Standing up from sitting in a chair
- Removing a garment, such as a fleece jacket
- Handling of plastic materials

For the removal of a sweater, voltages of > 20 kilovolts have been observed in dry air, and while performing experiments which tried to maximize the voltage, voltages of > 40 kilovolts have been measured while handling Nylon clothing materials. These extreme values do not indicate that each device should be tested to 25 or 40 kilovolts, but they are a reminder that voltages of > 25 kilovolts can occur in rather ordinary circumstances (removing a sweater on a dry winter day). In setting a test level, the manufacturer should consider:

- The likelihood of electrostatic discharges at a certain voltage level, which will depend on the surroundings, such as: consumers may use devices in a wooden house where the capacitance to ground is low (leading to higher voltages), in dry air during winter, in an automobile, or in an office environment.
- The consequences of the ESD (such as soft failure or damage).
- The usage of the device (safety-related, medical equipment, automotive, consumer electronics).

The test voltage levels in IEC 61000-4-2 (2008) are based on the synthetic fabrics line of Figure 62.

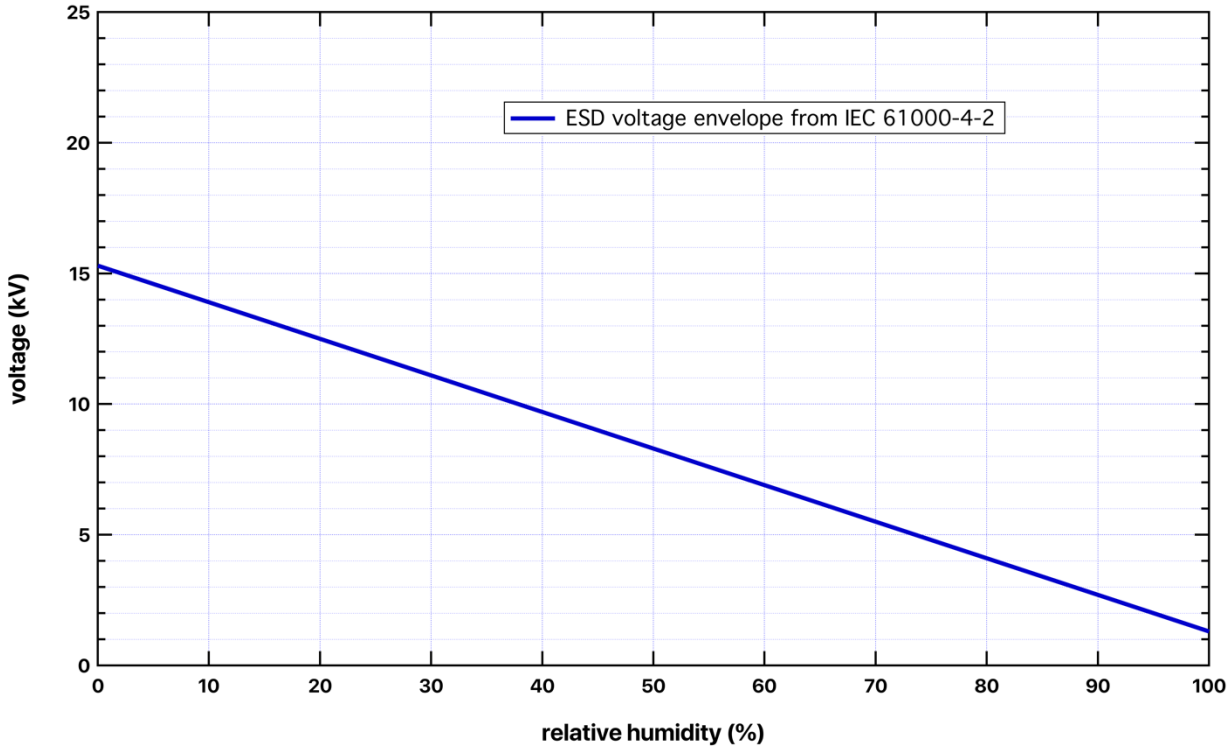


Figure 62: The maximum value of electrostatic voltage to which a person may be charged while in contact with synthetic fabrics (according to Figure A.1 of IEC 61000-4-2).

Note that there are no data points on this graph, nor references to sources, nor experimental information, nor any explanation of how this graph was made. So, an attempt was made to try and reproduce the experiment. Figure 63 shows the data from that experiment (red circles), the maximum voltage envelope of the data (green line), and the synthetic fabrics line of Figure 62 (blue line).

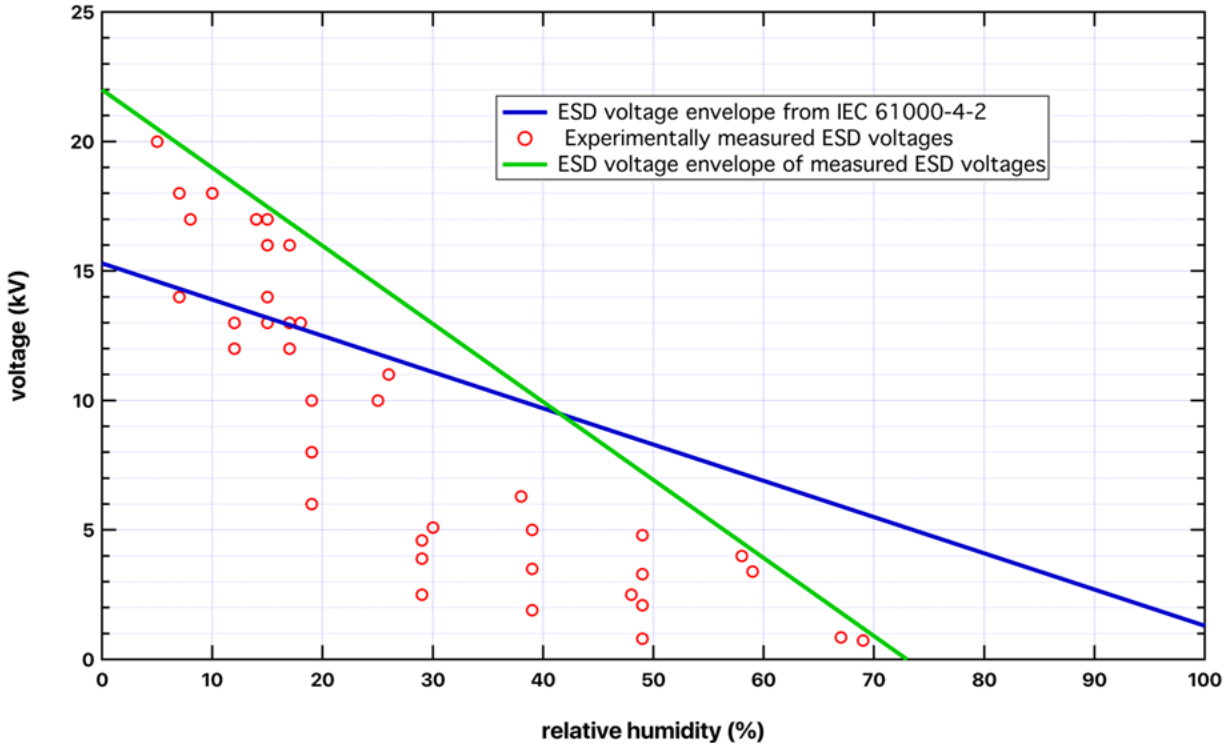


Figure 63: The measured values of electrostatic voltage to which a person may be charged after contact with synthetic fabrics (red circles), the linear envelope of these data points (green line), and the IEC 61000-4-2 maximum value of electrostatic voltage (blue line).

This experiment was done in an environmental chamber at 30 °C. The person charged themselves by putting on a synthetic fleece jacket, rubbing the jacket, then removing the jacket. The voltage on the person was measured with a Trek 341B non-contact electrostatic voltmeter with a range of 0 to 20 kilovolts and an accuracy of better than 20 volts. The lowest voltage data points at each humidity correspond to weak rubbing of the jacket, while the highest data points at each humidity correspond to aggressive rubbing of the jacket.

Note the significant differences between the results of this experiment (Figure 63) and Figure 62 of IEC 61000-4-2 (2008). In this experiment, at 70 % RH, no amount of rubbing would produce a body voltage greater than 1 kilovolt. According to Figure 62, at 70 % RH it is possible to produce a body voltage greater than 5 kilovolts. In this experiment, at 5% RH, it was easy to produce a body voltage greater than 20 kilovolts. According to Figure 62, at 5 % RH it is impossible to produce a body voltage greater than 15 kilovolts.

In summary, these experimental results suggest the test voltage levels in IEC 61000-4-2 (2008) are not realistic. It was decided to determine the voltages levels and frequencies that real handheld consumer electronics see in the hands of customers. A survey was conducted of smartphones, e-readers, and tablet computer users in the USA. The survey was planned and carried out with the assistance of a professional survey company. A total of 41,906 devices were surveyed, covering every state in the USA. Users were asked to estimate the length and frequency of sparks to their devices over the past year and describe if any type of device failure had occurred as a result. The ESD breakdown voltages were estimated from the reported spark lengths using the interpolated curve in Figure 64.

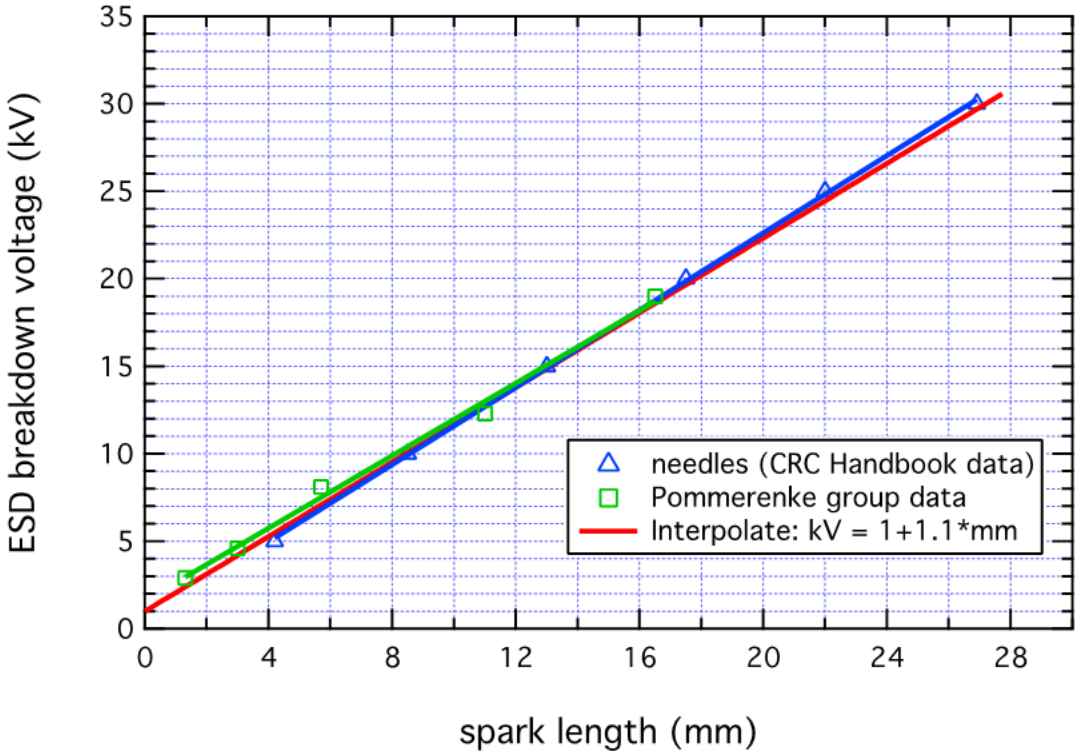


Figure 64: ESD breakdown voltage vs spark length.

The voltage and frequency data give the field ESD cumulative distribution shown in Figure 65.

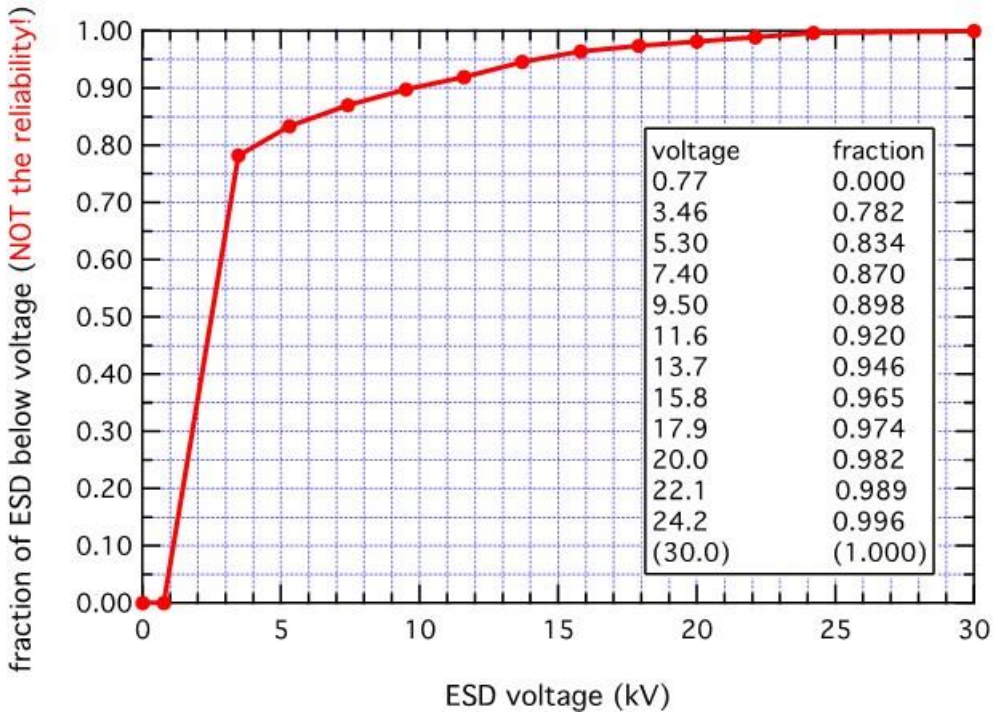


Figure 65: The cumulative distribution of ESD voltages in the field, based on a consumer survey of smartphones, e-readers, and tablet computers in the USA. The point at 30 kV is added as an estimate of the maximum field ESD.

These data show that ESD voltages greater than 20 kilovolts do occur in the field, and about 2 % of the field ESD is above 20 kilovolts. This is consistent with the experimental results shown in Figure 63. These data also show that about 5 % of field ESD voltages are greater than 15 kilovolts. These results show that testing to a maximum voltage of 15 kilovolts is neither realistic nor representative of field ESD. It is proposed to change the recommended air discharge test voltages to 4, 8 and 15 kilovolts, and, if covering rare extreme events is part of the quality goal, to test at 24 kilovolts.

8.1 Number of Test Points

The IEC 61000-4-2 standard (2008) specifies that each equipment under test (EUT) should receive at least 10 discharges at each test voltage level. No reasons are given for this specification. The field ESD cumulative distribution in Figure 65 shows that the probability of an ESD discharge to a EUT in the field decreases significantly with voltage. For example, the probability of an EUT in the field seeing a discharge between 0 and 5 kilovolts is about 16 times greater than the probability of the same EUT seeing a discharge between 10 and 15 kilovolts. These results show that doing 10 test discharges at every voltage is neither realistic nor representative of field ESD. It is proposed to do more test zaps at lower voltages and fewer test zaps at higher voltages. The optimum ratios were worked out by Renninger [Ren1992]:

$$\frac{N_i}{N} = \frac{\sqrt{f_i}}{\sum_{j=1}^{L} \sqrt{f_j}}$$

where:

i = *the test voltage number subscripts: V_1 = 4 kV, V_2 = 8 kV, etc.*
N_i = *the optimum number of test zaps at test voltage V_i*
N = *the total number of test zaps at all test voltages*
F_i = *the fraction of field zaps ∈ the voltage range $V_{i-1}V_i$*
L = *the maximum test voltage number, e.g. L = 4*

The IEC 61000-4-2 standard (2008) also implies that each test location of the EUT should receive 10 single discharges. This does not make sense. In the field, some locations on the EUT are touched much more frequently than other locations. Figure 66 depicts the data from the same consumer survey of smartphones, e-readers, and tablet computers in the USA.

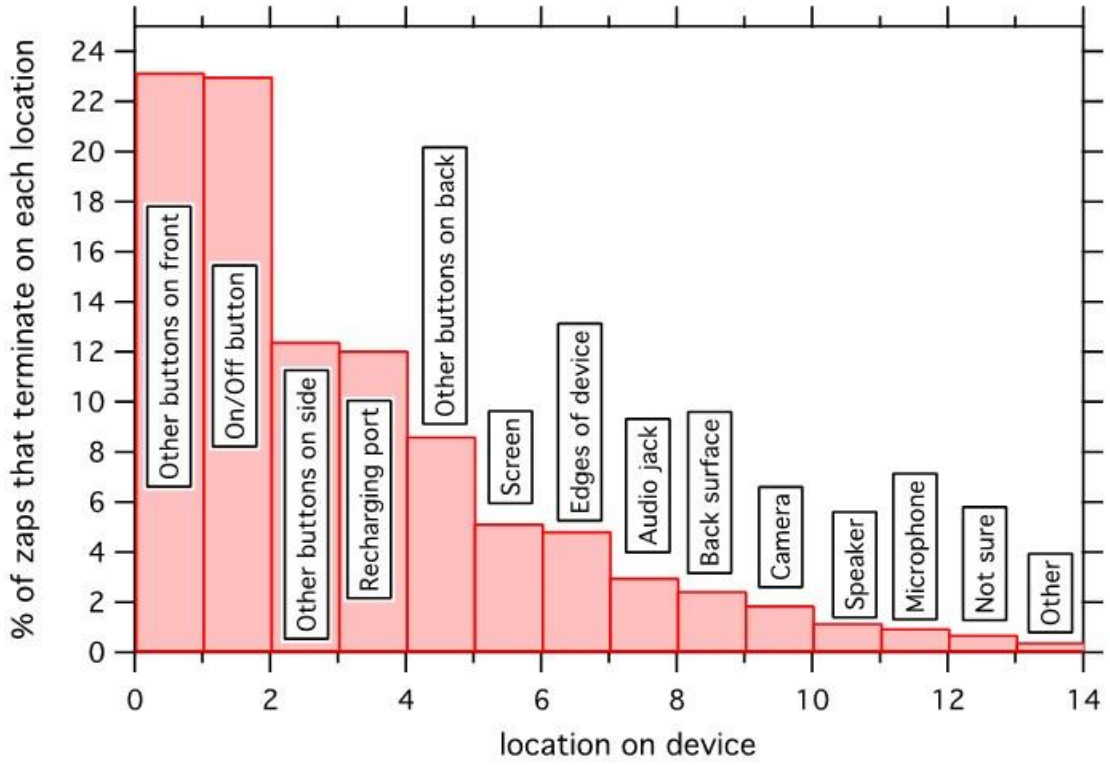


Figure 66: The frequency of ESD discharges onto different parts of handheld consumer electronics products in the field, based on consumer surveys of smartphones, e-readers, and tablet computers in the USA.

These results show that doing 10 discharges at every test location on the EUT is neither realistic nor representative of field ESD. Every test engineer will intuitively select ESD test points. Connectors and user interface devices, such as screens, knobs etc. will intuitively be given priority. This methodology substitutes the intuitive test point selection by a systematic approach to enhance the correlation between field ESD locations and test ESD locations. If the information on locations that are subjected to ESD by the user is available, it is proposed to do more test zaps at test locations that see more field zaps and fewer test zaps at test locations that see fewer field zaps. To simplify and generalize, consider four groups of locations as a useful approach:

- Group 1 (82 % of all zaps): Openings that customers will touch frequently: buttons, USB jacks, audio jacks, charging ports, etc.
- Group 2 (7 % of all zaps): Openings or seams that customers will touch infrequently: speaker holes, microphone openings, housing/mating seams, etc.
- Group 3 (5 % of all zaps): The screen (both touch and non-touch screens)
- Group 4 (6 % of all zaps): Surfaces: the back of the device, etc.

Here it needs to be reiterated that this is a concept that can be used as a quality tool in developing ESD test requirements and predicting field failure rates within a company. This is not intended to become mandatory nor to be included in the IEC 61000-4-2 test standard.

The IEC 61000-4-2 standard (2008) defines a test for the performance of electronic equipment when exposed to predefined electrostatic discharges in a specified laboratory environment but says nothing about how these test results correlate with the performance of the same electronic

equipment when exposed to real electrostatic discharges in the field. Electronic equipment manufacturers and users need quantitative estimates of the reliability of electronic equipment when exposed to real electrostatic discharges in the field, before this equipment is deployed in the field. Renninger [Ren1993] developed a technique for doing this. Applying his work to the ESD survey data gives:

$$R_{lf} = 1 - 0.1765[(\sum_{i=1}^{L} f_i\, p_{ui}) + f_{max} p_{umax}]$$

where:

-R_{lf} = *the predicted lower limit on the first-year field reliability*
-0.1765 = *the average number of zaps per smartphone/ereader/tablet per year ∈ the field (the survey data)*
-i = *the test voltage number subscripts:V_1 = 4kV, V_2 = 8kV, etc.*
-L = *the maximum test voltage number, e.g. L = 4*
-f_i = *the fraction of zaps ∈ the voltage range $V_{i-1}V_i$ ∈ the field (survey data)*
-f_{max} = *the fraction of zaps above V_L ∈ the field (the survey data)*
-p_{umax} = *the upper limit on the probability of device failure at $V>V_L$,∧*
-p_{ui} = *the upper limit on the probability of device failure at V_i, obtained by solving:*

$$\sum_{k=n_i+1}^{N_i} \frac{N_i!}{k!\,(N_i-k)!} p_{ui}^{k} (1-p_{ui})^{N_i-k} = C,$$

where:

-n_i = *the number of failures at voltage Vi*
-N_i = *the number of discharges at voltage V_i,∧*
-C = *the one – sided confidence level*

An ESD Calculator was written that helps plan an ESD test, analyzes the test results, and predicts the field reliability at a chosen confidence level. To obtain and use this calculator:

1. Download and install the free CDF Player:
www.wolfram.com/cdf-player/
2. Download the free ESD Calculator:
https://drive.google.com/open?id=1XNc7GlOnGvc-6785Plpx8klk0lSY7pE5
3. Start up the CDF Player,
4. From within the CDF Player, open the ESD Calculator, and
5. Follow the directions in the ESD Calculator.

8.2 Reducing the Variation of Discharge Currents during Air Discharge Testing

In the interest of improving the reproducibility of air discharge during IEC 61000-4-2 ESD testing, different methods are investigated that reduce the variation of the spark current during air discharge. As the variation is caused by the interplay of the statistical time lag and the approach speed, methods

are investigated that provide initial charge carriers for the avalanche initiation at the beginning of sparking. These methods include ionizers, cold plasma, humidity, exposure of the electrodes to UV light, different electrode materials, and surface shapes. While most of these methods reduce the variations of the spark currents, only some can be implemented during testing. The strongest effect was achieved by using cold plasma and by one surface material found in a gasket.

8.2.1 Background

The IEC 61000-4-2 ESD standard describes both air discharge and contact mode testing. Contact mode does not reflect ESD outside the test lab, but its reproducibility is better. Further, the IEC 61000-4-2 standard does not contain a calibration method for air discharge. This, and the low reproducibility of air discharge, led to suggestions to remove air discharge from the standard's mandatory requirements. However, if this step would be taken, many DUTs would not be tested for air discharge. As most critical test points are non-conducting (knobs, switches, displays, gaps in plastic enclosures, wires) the ESD standard would lose its ability to hold ESD induced field failures to a low level.

Introducing a calibration for air discharge of ESD generators has been investigated by multiple authors [Ish2016, Yan2018]. The methods either try to stabilize the spark, or, avoid having a spark. The method proposed in [Yan2018] and as discussed in Section 7.4 measures the step response of the ESD generator in air discharge mode. As this fully characterizes the ESD generator, it provides a suitable calibration method of ESD generators in air discharge mode. Practical testing requires further considerations. The waveform is not only determined by the linear step response of the ESD generator, but also by the time dependent spark resistance.

It is known that ESD air discharge currents vary strongly from ESD to ESD even if the approach speed, electrode and voltage etc. are kept constant. This is caused by the interplay of the statistical time lag and the approach speed. This phenomenon is well understood [Pom1995, Pom1993].

Every spark gap has its static breakdown voltage. This is the minimal voltage at which a breakdown can occur. For homogeneous fields the static breakdown voltage can be calculated from Paschen's law. This leads to 2.8 mm at 10 kilovolts and 1.1 mm at 5 kilovolts. If sharp edges or sparks gliding on plastic surfaces are involved the static breakdown voltage cannot be determined by Paschen's law [Zhou2018]. The core aspect of the static breakdown voltage is that a breakdown can occur, however, it does not necessarily happen right away. To initiate the spark, initial electrons are needed [Mor1953, Mee1978]. If there are no initial electrons and the electrodes are approaching, then the gap can close further until a breakdown occurs. This is illustrated in Figure 67. If the gap closes, e.g., at 10 kilovolts from 2.8 mm to 2 mm before a breakdown occurs, the current will rise faster, and reach higher peak values once the breakdown occurs. This is caused by the increased field strength within the gap. Examples of such measurements are shown in Figure 68.

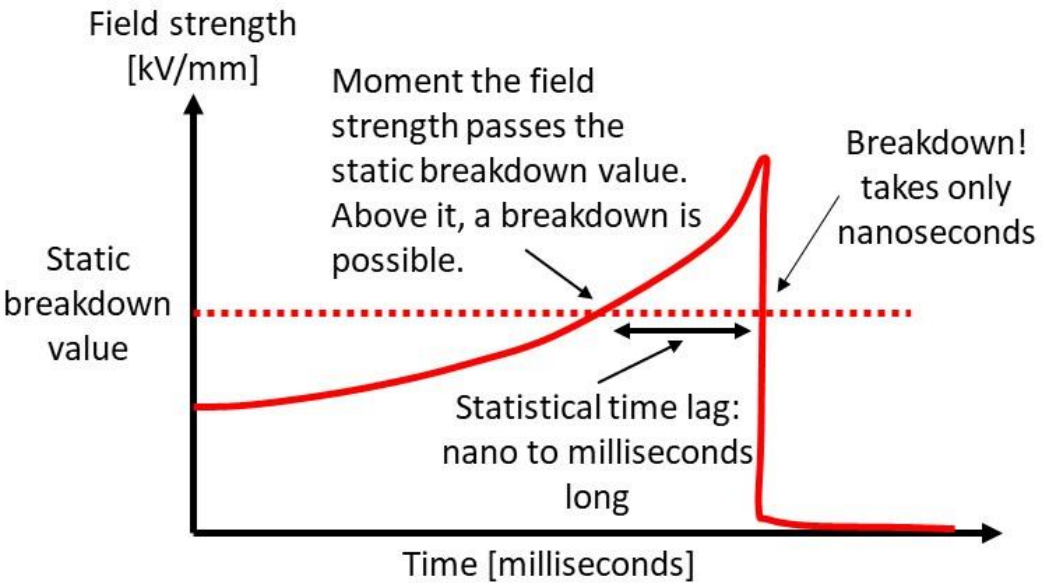


Figure 67: Graphical explanation of the statistical time lag and its influence on the breakdown.

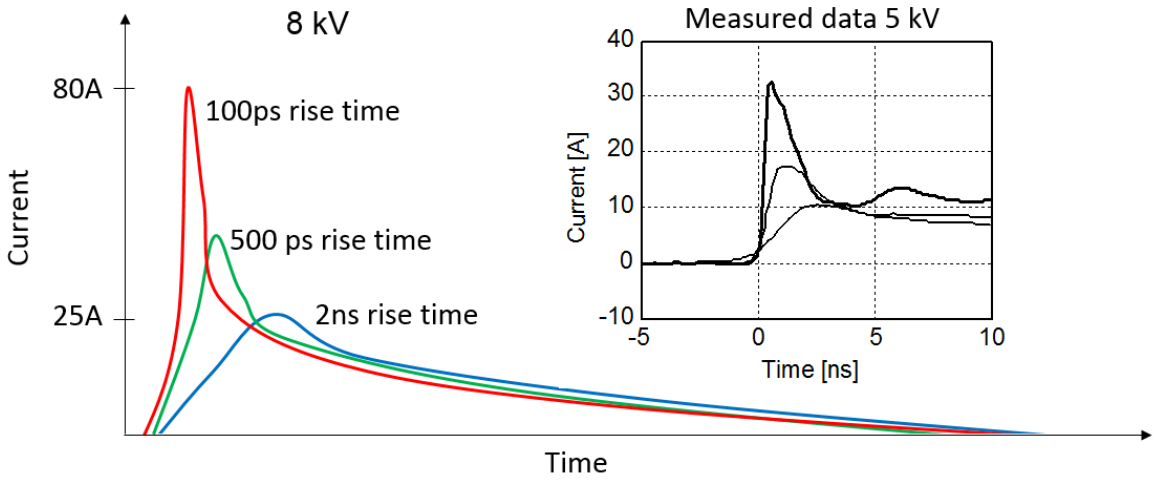


Figure 68: Human discharge currents from a person holding a metal piece for different spark lengths. Left: Illustration, Right: Measured currents.

In an environment in which initial electrons are widely available, the gap will breakdown once the field strength reaches the static breakdown field strength. If the operator repeats an air discharge at typical approach speeds of 0.01~1 m/s the interplay of the statistical time lag and the approach speed can lead to large variations of the discharge currents. This is caused by variations of the spark length. If this effect is observed or not depends on the voltage, and the availability of initial charge carriers that can initiate the avalanche breakdown of the spark.

If clean metal electrodes are used, e.g., a stainless-steel air discharge tip of an ESD generator and the ESD current target, the variability is strong for voltages larger than 2 kilovolts and diminishes above 15 kilovolts [Fri1999]. The smaller variations observed at the low end are probably caused by the fact that discharges at lower voltages are not gas discharges, but discharges that take charge

carriers from the metal surfaces, and at higher voltages the edges at the current target will provide initial charge carriers.

Initial charge carriers can also be provided by a variety of mechanisms that are discussed in greater detail in this white paper. Examples are humidity, sharp edges, UV light etc.

While a proposed method that has the potential to be a calibration method for ESD generators in air discharge exists [Yan2018], it is still desirable to reduce the discharge to discharge variations during testing. One approach is to create an environment that has a large density of initial charge carriers. These will initiate the spark once the field strength reaches the static breakdown value of the gap. However, this may be impractical during testing, and a lesser goal can improve the testing. Any modification of the test method that reduces the likelihood of those electrostatic discharges that have extremely short sparks will improve the test result uncertainty.

8.2.2 Experimental Setup

In this white paper, a variety of methods are investigated that can improve the repeatability of the ESD discharge. All of the methods provide initial charge carriers to increase the likelihood that an ESD occurs at a spark gap distance that is at, or not much shorter than, the static breakdown distance. The experimental investigation captures discharges from an ESD generator to a current target, or from a modified current target having a sharp point. The current is analyzed by its peak value, variability, and maximal current derivative. Then, different methods are used to influence the spark development, such as shining UV light onto the gap to create initial charge carriers via the photoelectric effect.

This white paper compares the different methods and identifies solutions that will improve the repeatability of air discharge.

The variability of the spark current is caused by the interplay of the statistical time lag and the approach speed. An obvious choice would be to reduce the approach speed, such that the spark will occur at the distance which is given by the static breakdown value. However, this would require very slow speeds, often less than 1 mm/sec [Fri1999]. The alternative is to create a sufficient number of initial charge carriers such that the breakdown occurs at the static breakdown distance, or at distances that are not much shorter.

There are a variety of methods to create initial charge carriers. These can be externally provided, or be delivered by the electrode itself.

Methods that provide ions from the outside are listed below:

- Ionizer: An ionizer provides a stream of ions. These can be either charge balanced, negative, or positive ions that dominate the ion flow
- Cold plasma gun: A cold plasma is a non-equilibrium plasma. Its electron temperature is much larger than the ion temperature. Thus, it is not physically hot, and can be touched. Cold plasma [Plasma] is often used to disinfect surfaces or to activate plastic surfaces before gluing them. The cold plasma gun is similar to an ionizer, but the ion density is much larger.
- Radioactive materials: An alpha or beta decay material will create initial charge carriers. This is often used in smoke detectors and in low jitter (Krypton filled) spark gaps. Due to the complexity of handling radioactive material, this was not investigated in this study.

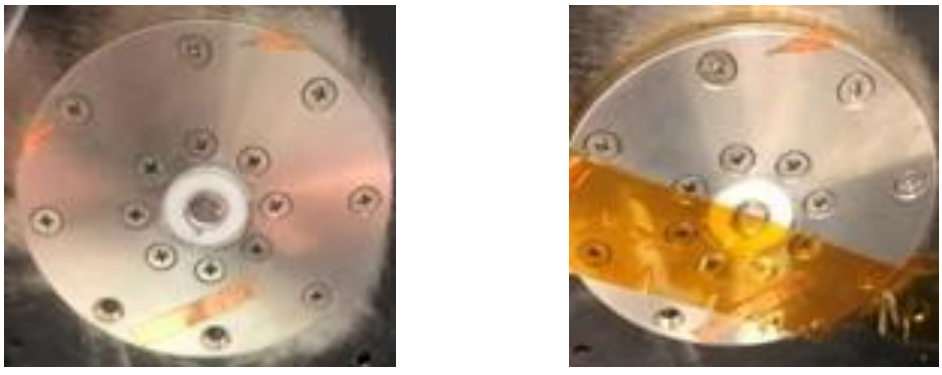
- UV light or laser: The photoelectric effect will create charge carriers. Here, either a low pressure Hg lamp or a UV laser can be used. Both emit photons in the range of 240 nm. However, a laser can focus a much larger photon density on the gap and can influence the spark development strongly.
- High humidity: It is known that water molecules attract charge carriers as the water molecule is highly polar. In a rather low field strength, the charge carriers can detach and initiate a spark. This effect causes the humidity to have a very strong impact on the statistical time lag. Thus, applying moist air may reduce the time lag, and thus stabilize the spark development [Gos1985].

Methods that provide charge carriers from the electrodes are listed next:

- Graphite ESD generator tip: It is known that graphite has a strong electron emission even at rather low field strength. It has been used as fast reacting overvoltage protection spark gap since the early days of telegraphy [Lev1982, Sta1998].
- Gaskets: It has been observed that different gasket materials, such as fabric over foam gaskets, help to initiate a spark at lower field strength. The gasket material is glued, using a conductive glue, to the ESD generator tip. Besides such gaskets, other surfaces such as steel wool, copper wool etc., have been investigated.

8.2.3 Measurement Setups

The experimental setup captures the discharge current. At first, the data is analyzed by visually inspecting the variability of the waveforms. Numerical analysis quantifies the variation of the maximal time current derivative (max (di/dt)) of the discharge current. This measure was selected as it is closely related to soft failures and the rise time of the pulse. Three different electrode setups were used, see Figure 69. The first uses a standard ESD current target, the second adds a pointed tip to the target, and the third partially covers the target with Mylar tape. The second setup was selected as most DUTs will have sharp edges, e.g., at the PCB. The last setup was selected because practical air discharge testing nearly always approaches plastic or glass surfaces to allow a spark to glide on the surface of the insulator and possibly reach a grounded metal part. It was selected to confirm that such discharges lead to slower current derivatives compared to discharges in air.



(a) (b)

Figure 69: Measurement setup: (a) Current target mounted into a shielding enclosure. (b) Mylar tape partially covering the current target to mimic structures having the spark travel along a plastic surface.

The discharge currents were measured by the current target and an oscilloscope inside a shielded enclosure. The bandwidth of the measurement system is mainly limited by the oscilloscope

bandwidth. A 2 GHz oscilloscope was used to capture most waveforms. Select data, used for the statistical analysis in Section 8.2.4 was captured using a 13 GHz oscilloscope.

8.2.4 Measurement Results - Current Waveforms

The fastest rising currents are obtained if the statistical time lag is long at higher approach speeds. The approach speed was manually kept approximately constant around 10 cm/sec.

A 13 GHz oscilloscope was used to obtain the reference data when the ESD generator discharged to the flat surface of the current target (see Figure 70). The test was repeated 100 times. The test environment was at 20 % relative humidity and 23 °C. A low humidity was selected as this aggravates the problem of repeatability of the air discharge. Any effect observed by a method to improve the spark repeatability would be even more efficient at higher humidity.

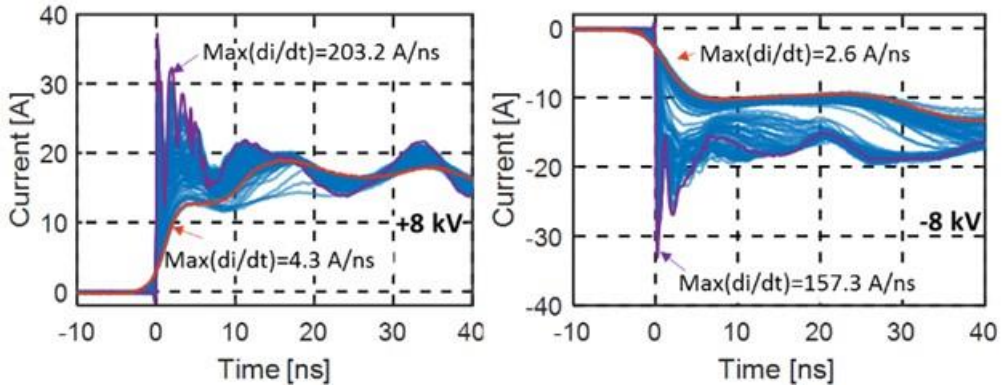


Figure 70: Current waveforms without using any methods to stabilize the waveform at +8 kV and –8 kV. 100 waveforms have been captured and the maximal current derivative extracted.

The maximal current derivative is used for the analysis as the maximal current derivative often correlates to the soft failure threshold for electronic systems. The figure also shows the range of the maximal current derivative (di/dt) for each discharge. They are obtained from either 100 or from 30 repeated measurements. The initial investigation using 30 discharges provided preliminary judgements on the effectiveness of the methods.

As it is not possible to present all the data, a selection was chosen such that the dominating effects are illustrated. Figure 71 shows current waveforms obtained while exposing the spark gap to cold plasma. The maximal current derivative is limited in a small range from ~2 A/ns to 4 A/ns.

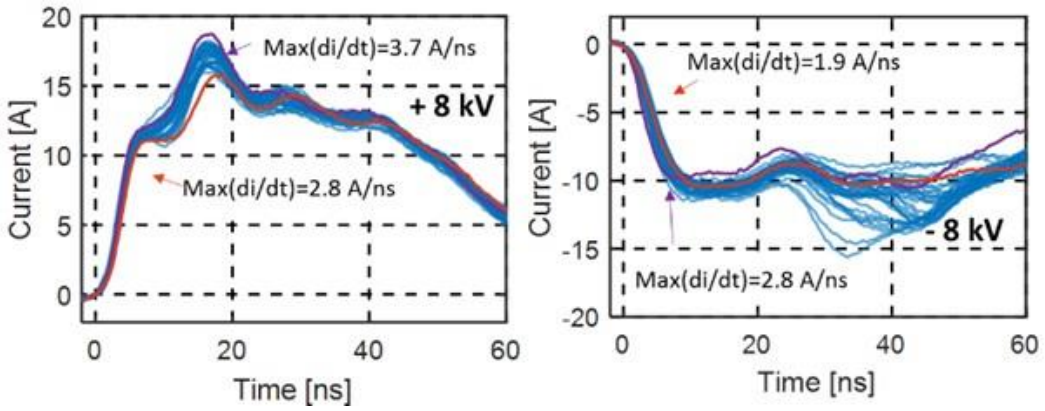


Figure 71: Current waveforms using cold plasma to provide external initial charge carriers at +8 kV and -8 kV.

Commercial ESD generator tips are usually made from stainless steel. Polished stainless steel has a low electron emission for a given field strength. In contrast, graphite is a strong emitter [Lev1982, Sta1998]. A graphite tip was machined to replace the stainless-steel tip. The current waveforms using the graphite tip are shown in Figure 72. The graphite tip only helped to stabilize the waveform at negative polarity. This can be explained by graphite being an electron emitter.

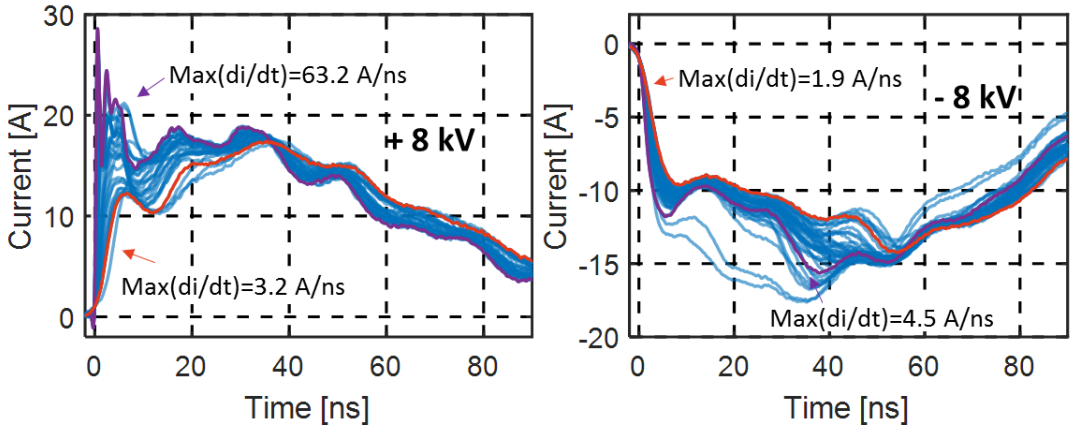


Figure 72: Current waveforms using the graphite tip at +8 kV and -8 kV.

Another data set presented here was obtained using a gasket, shown in Figure 73 with a picture of the gasket material used shown in Figure 74. This fabric over foam gasket covered the ESD generator tip during the discharges. It greatly stabilized the spark initiation. With respect to the test standard, it would be an easy change to modify the ESD generator air discharge tip by covering it with a gasket. The exact mechanism and surface properties of this gasket have not been clarified yet.

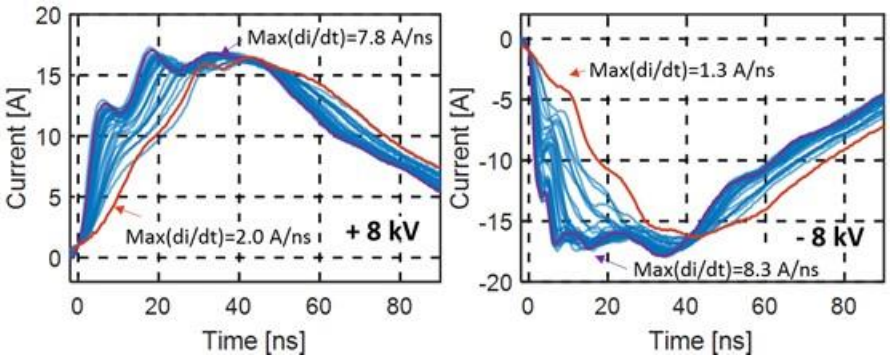


Figure 73: Current waveform obtained using a gasket to cover the tip at +8 kV and -8 kV.

Figure 74: Gasket Material Larid cf100

8.2.5 Maximal Current Derivative Distributions

The data shown in the Figures 70 to 73 give a visual impression of the variations and quantifies the max (di/dt). A statistical analysis of the distribution of the current derivative values gives further insight into the effectiveness of the methods investigated.

It had been shown that spark discharges having spark lengths close to the static breakdown gap distance have current derivatives of a few A/ns for voltages relevant to system level ESD testing in the range from 2 to 15 kilovolts [Pom1995, Pom1993]. In air discharge testing of an ESD gun against an ESD target, the current derivative may reach hundreds of A/ns. During product testing, the range of variation will depend on the shape of the surface and other parameters. However, if the air discharge occasionally leads to a very large max (di/dt) value, failures may occur that are hard to reproduce. Thus, it improves the test result uncertainty if the statistical distribution of the current derivatives does not contain very fast rising events. The methods used to stabilize the spark initiation have been statistically analyzed by observing the distribution of max (di/dt) with special attention to very fast rising electrostatic discharges.

It is not possible to show all distribution functions (multiple voltage levels and both polarities). Thus, only those have been selected which indicate successful stabilization of the spark initiation. The data shown in Figures 75 and 76 are based on 100 discharges. The green bar shows the distribution using the stainless-steel air discharge tip. The current derivatives are broadly distributed and include discharges having > 100 A/ns max (di/dt). This data can be considered as the reference, as the data is captured using the method outlined in the IEC 61000-4-2 standard. A graphite tip was

machined having the same dimensions as the stainless-steel tip. Graphite was selected as it is known to have a strong electron emission under rather low surface field strengths [Lev1982, Sta1998]. For positive voltages, the graphite tip (blue bar) removes most of the very fast rising discharges, but the distribution is still rather broad. The effect is much more pronounced for negative charge voltages. Here, the initiation is clearly driven by electrons from the tip. Graphite being a good electron emitter led to discharges having low max (di/dt) values. For negative charge voltages, using a graphite tip was nearly as effective as using cold plasma (not shown in the figure). Another method selected for Figures 75 and 76 was the usage of a gasket. This foam over fabric gasket (2 mm thick) was used to cover the air discharge tip. The surface materials and microscopic structure of the gasket material have not been investigated. The gasket material stabilized the spark initiation strongly, as is shown by the red bars in Figures 75 and 76.

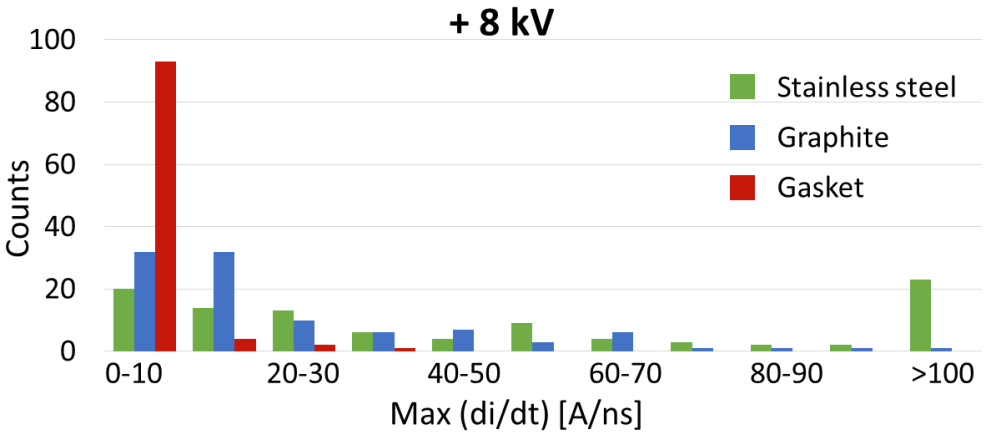


Figure 75: Maximal current derivative distributions for different tip materials at + 8 kV.

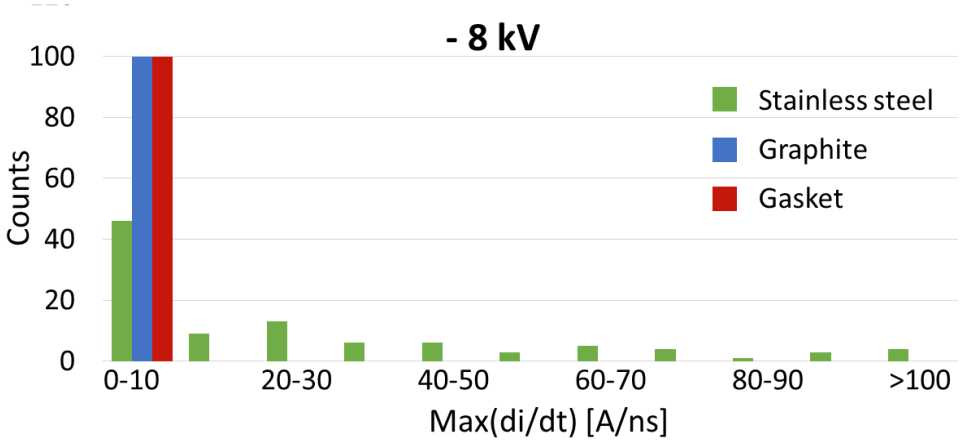


Figure 76: Maximal current derivative distributions for different tip materials at - 8 kV.

8.2.6 Comparison of the Methods

This study forms an initial investigation into methods that might be used to improve the repeatability of an air discharge in the IEC 61000-4-2 standard. The data was obtained on a limited

number of discharges in just one humidity condition. However, the data already indicates possible paths to improve the repeatability. The data is summarized in Table 6.

The maximal current derivative ranges are shown, and the effectiveness is compared for each method at positive/negative 8 kilovolts. All methods, except using graphite for positive voltages, show some effect on the rise time stabilization. However, the effectiveness varies, and the complexity of implementation varies greatly. According to this limited data set, the methods that provide external charge carriers can limit the max (di/dt) to below 10 A/ns. But those methods may not be practical for engineering tests. For example, water mist helps to stabilize the waveforms, most likely due to the electron affinity of water molecules. However, one cannot expose a DUT to water mist. The graphite only helps to stabilize the waveform for the negative voltage.

The strongest effect was achieved by exposing the gap to cold plasma during the discharge. However, due to the creation of NOx gases, it would require good ventilation. The cold plasma may also interact with circuits, because it is created by a high power ultrasonic piezo device.

The UV laser used in this experiment provided 1 mW of optical power. However, the wavelength of 240 nm can cause deoxyribonucleic acid (DNA) damage if human skin is not protected. Similar arguments limit the use of low-pressure mercury lamps. Here, a 150 W lamp (AC power consumption) was used.

Ionizers may provide a practical method, as well as covering the ESD generator air discharge tip with a fabric over foam gasket. Further investigations are needed to determine if these are good options.

Table 6: Effectiveness Comparison for Different Methods

Method	**Max(di/dt) [A/ns]**		**Method / Comment**
	At +8 kV	***At -8 kV***	
Stainless steel reference	4.3~203.2	2.6~157.3	Reference based on IEC 61000-4-2
Cold plasma	2.8~3.7	2.0~3.8	Effective, creates NOx
Ionizer	2.7~4.0	1.6~3.1	Effective
UV laser	2.9~5.3	1.8~3.6	Effective, avoid eye and skin exposure
Moist air	3.2~4.5	0.7~3.3	Humidity very high, fog conditions
Gasket	2.0~7.8	1.3~8.3	Effective and easy to implement
Graphite	3.5~174.9	2.5~8.7	Only effective for negative voltages
Mylar tape	1.3~4.5	1.5~13.9	Depends on the DUT geometry, not practical as change to the IEC 61000-4-2 test standard

8.2.7 Summary

This section improves understanding of air discharge testing, its related problems, and may lead to an improved IEC 61000-4-2 standard. The research points at possible solutions to the problem of bad reproducibility in air discharge testing. Multiple methods to stabilize the spark initiation during air discharge testing have been investigated. Testing compared the maximal current derivative during the air spark to the reference event, which is the discharge between the ESD generator's air discharge tip and the ESD current target. All methods, such as UV exposure, cold plasma, using a graphite tip, high humidity, and modified surface materials, improved the reproducibility. However, only the usage of an ionizer and modified surface materials may be useful in ESD testing.

8.3 Testing Inside a Shielded Room

ESD testing is often performed inside a shielded room. The shielding of the room has no effect on the testing, reflections of the electromagnetic waves in the room are also not critical as the distance from the ESD generator to the DUT is much smaller than the path from the ESD generator to the walls and then to the DUT. However, the grounded metal walls change the capacitance of the HCP. A larger capacitance of the HCP to ground may influence the test results if the HCP to ground voltage is relevant. For example, if a keyboard is tested by discharges to the HCP (indirect ESD testing), then the ESD generator will charge the HCP to a voltage which is determined by the capacitance ratio of the ESD generator's internal capacitance and the HCP to ground capacitance. The keyboard, here assumed to be grounded, will see a different E-field. The capacitance of the HCP to ground is also affected by any DUTs or support equipment that are placed upon it. If this equipment is grounded, e.g., via a power cord, the capacitance of the HCP to ground will be increased by the test equipment that is placed upon the HCP. This change is part of the specific test setup, and not of concern. However, increased capacitance due to the proximity of a metal wall should be avoided.

In a display-down test situation, a phone for example, the capacitance from a small phone to the HCP is in the range of 50-100 pF, this is the same range of the HCP to ground capacitance. If there is a discharge to the phone's back side, then the voltage across the display (the voltage reached after ringing is over, so the voltage after a few nanoseconds) is determined by the phone to HCP capacitance, the ESD generator's internal capacitance and the HCP to ground capacitance. In this case the voltage across the display will vary with HCP to ground capacitance (and with the flatness of the dielectric insulator).

For most DUTs, the effect of the HCP to ground capacitance may not be critical as they do not react to discharge to the HCP. However, an adequate distance to metal walls should be maintained.

8.4 Humidity

Humidity only affects air discharge, contact mode is not affected. The charge decay on the surface may be affected, however, within the 35-65 % RH range this may not be such a strong effect. Secondary ESD may also be affected. For homogeneous field discharge structures, the effect may be large, but most practical secondary ESD structures will have sharp edges, or plastic surface guided spark paths. Thus, the effect of humidity on the secondary ESD will be low, as the time lag

is dominated by the edges or plastic guided surfaces [Wan2014]. Still, the present temperature/humidity range allows rather large variations which may affect air discharge.

8.5 Charge Removal

The underlying idea of the IEC 61000-4-2 test standard is that every ESD is unaffected by a previous discharge. This relates to software; all error corrections should be completed before the next ESD is applied, and to electrostatics; any charges introduced from a previous ESD should be removed.

Often there is confusion about the best method of charge removal, for example:

- If an ionizer is used during the testing to remove charges after the ESD, does the ionizer change the air discharge spark? Does it change the secondary ESD occurrence or severity?
- How long will an ionizer take to remove the charges?
- Can one connect a high impedance ground strap to the DUT while testing? Or does one need to remove the ground strap for each discharge?

With respect to attaching a ground strap during testing to the DUT, one should consider two possible effects of the ground strap:

- The attached conducting structure may affect the current distribution during the ESD. This will be the case if the wire has a long section before its first high impedance resistor is included into the wire. A wire < 5 cm should not cause any concern as the capacitance of a < 5 cm wire to ground is probably < 2 pF and the propagation delay along the section is several hundred pico-seconds. Thus, a wire that contains a high voltage, high impedance resistor after < 2 cm should not affect the current distribution during testing in any significant way and it can be left attached during testing. An alternative is to use a conductive grounding using a high impedance wire, such as a carbon fiber. For example, if such a wire has a resistance of >10 kilohm/m it is most likely invisible from an RF point of view. Such wires are used in EM-field sensors to connect the local RF detection diode's DC voltage to an analyzing instrument.
- The attached wire will change the time constant of the discharge of the DUT. This is the goal of introducing the wire. However, if there is secondary ESD in a power supply then it may take time for the secondary ESD to develop. Thus, the time constant should not be too small. A time constant of 1 ms will not influence any secondary ESD. A value often selected is 1 megohm, however, if the DUT to ground capacitance is 100 pF, then this leads to 0.1 ms time constant, a value a little bit smaller than the suggested value. For that reason, a discharge resistance value of 100 megohm seems more appropriate. The 100 megohm can be created by placing 1 megohm close to the DUT and 100 megohm at the other end of the wire. This may lead to a mechanically more suitable structure as a smaller 1 megohm can be used; the voltage drop across this resistor will be rather small due to the series connected circuit. The secondary ESD case may need further explanation. Consider a DUT that is only "grounded" via a power-brick which is connected to a 2-wire power cord. In this case there may be no DC return path from the DUT to the ground. Now the ESD to the DUT will increase the voltage inside the power brick which may lead to a breakdown inside the power brick. This is a commonly observed secondary ESD situation. The power brick may be damaged and fail, or worse, overvoltage the DUT.

After considering the effect of charge removal methods that are applied during the injection for their possible effect on the ESD current it is suggested to simply use a static voltmeter to test if the charge removal method used (e.g., wire, brush, ionizer) is enough. If the static meter shows that the charges are removed to < 10 % of the initial charge value one can reasonably assume that the remaining charge has no effect on the next ESD pulse.

8.6 Multiple Pulse ESD

Although it is known that a real ESD often consists of a series of pulses, it is reasonable to base a test standard on single pulses independent of each other. Due to software correction and recovery it is plausible to argue that those series of pulses with millisecond time spacing will act differently than pulses which have seconds of time spacing. One needs to consider two aspects:

- Multiple pulses mainly occur if discharges from the skin are considered, discharges from a metal part usually have one dominating pulse and much smaller pulses which follow. Human-metal pulses are much more severe than HBM pulses, thus, it is reasonable to base the testing on the more severe case although it shows mainly one pulse
- The fact that an air discharge often consists of a series of pulses has been well documented. In general, the first discharge transfers most of the charge, it has the longest rise time and the largest peak value. Later discharges have faster rise times, but lower peak values. The reason for having multiple discharges is that the spark may extinguish if the current falls below a value on the first discharge. As the finger approaches the spark re-ignites at a lower voltage. The initial spark may have created a hole in the insulation of the skin, such that the rise time is faster upon re-ignition.

8.7 Documentation

8.7.1 Discharge Current

An advanced ESD system level test setup captures the discharge current during testing. Here a current clamp, such as an F-65/F-65A, is a good choice for capturing the current with sufficient bandwidth, and capturing the current using a flat frequency response such that the voltage shown by an oscilloscope can be expressed as current by simply multiplying it by the probe's transfer impedance. Any probes having a strong frequency dependent transfer impedance in the relevant frequency range from about 1 MHz to 1 GHz may require a more complex deconvolution to convert the captured voltage to the current waveform.

The current measurement serves the following purposes:

- It can be used to verify the ESD generator's performance prior to ESD testing. It is suggested to test at a low voltage, such as 250 volts, and at the highest voltage of 25 kilovolts. The two voltages are suggested as the typical failure mechanisms in the high voltage relays can cause either low or high voltage waveform problems. If the relay is worn, thus, its contacts have eroded over many ESD pulses, the low voltage waveform changes. However, the waveform at 4 kilovolts for example, may still be OK. If an insulation problem occurs in the ESD generator it is visible at the high voltage setting. Thus, these two voltage levels cover the most common failure types in ESD generator relays.

- If a DUT failure is observed during testing and the waveform is recorded, much better data is available for root cause analysis. For example, in an air discharge, it is quite common that the waveform will vary strongly. Thus, if the waveform is known which caused a failure it may help to understand the reason or the correlation to ESD test levels. This knowledge will also help in understanding spark-less ESD discharges as they occur on displays and provide information in disputes about passing / failing ESD tests between OEM manufactures and system integrating companies.
- Secondary ESD can be detected from the discharge waveform.

8.7.2 Video Recording

A problem often seen is a dispute between an OEM and a system integrator about passing or failing an ESD test. While there can be many reasons for test result variation, it is certainly not helpful if the test documentation is insufficient. It is known that the approach speed, and the angle of the ESD generator, routing of cables etc. can all affect test results. To improve the documentation, add a video recording to the ESD testing. Labs have placed video recording equipment on flexible arms such as the ones found in dentist office. This easily allows moving the camera to the region of interest. The camera will then record:

- Test setup
- ESD generator approach and location
- Parts of the DUT response.

These systems can be foot activated, such that the recording only captures the relevant seconds. If no error occurred, the recording may be disregarded. Such a system should be combined with a current measurement using a current clamp around the tip of the ESD generator, or at least on the ground strap. This captured current could then be correlated with the failure, such that the test report shows the video, the current waveform of the ESD that failed the DUT and possibly the DUT response.

8.8 Robotic ESD Testing

ESD testing can be performed by hand, robotically supported hand testing, and fully automated. In hand testing the operator will perform the testing and observe the DUT for failure indications. In robotically supported testing the robot will perform the testing. However, the operator will observe the DUT for failure indications. In fully automated ESD testing the robotic system will perform the testing, DUT supervision, DUT reset etc. See Figure 77.

Figure 77: Robotic IEC 61000-4-2 test system (courtesy of API, www.amberpi.com)

8.8.1 Advantages of Robotic Testing

Repeatability

Air discharge testing depends strongly on the length of the arc. The length of the arc can vary significantly even for the same test point and at the same voltage. Those variations are partially statistical in nature, but also are influenced by the way the approach is performed. The rise time will be lower, and the peak values will be higher on average for faster approach speeds. Some careless people even drag the charged air discharge tip across the product (being in contact with the plastic surface) to see if a discharge occurs. This is a very risky practice, as this can lead to an unrealistically low air discharge rise time. It is important to control the approach speed (straight to the point of expected discharge), and to control the angle that the ESD generator is held.

The robotic system allows every test parameter, such as, approach speed, angle and discharge point, to be precisely controlled and accurate.

Test depth

The advantages in test depth mainly come from a large number of consistent discharges. The number of zaps per test point is set to 10 by IEC 61000-4-2. There are brief periods of time in which a DUT is much more sensitive to ESD, and ten discharges is a very low number to capture rare failures (or windows of opportunity) that happen only at certain condition of a DUT during normal operation. A larger number of discharges (in the range of 100) at each test point with good repeatability provides more statistically reliable test results.

A DUT is usually controlled by a DUT controller that sets the DUT in many different modes of operation. Automated robotic testers enable tests of such various modes of operation without interruption or skipping some modes, which happens frequently during manual tests.

The voltage is often set in large increments, like 2, 4, and 8 kilovolts and only pass or fail is reported. It is important to know pass or fail, but it is just as important to know the failure level. Classifying pass or fail based on a large test voltage separation can cause inconsistency in the passing (or failing) level. For example, if a DUT's real passing voltage is 8010 volts. It can pass at one test lab, but easily fail at a different test lab.

Documentation
All test actions can be recorded automatically and pulled out as necessary. This can help in understanding correlation analysis of failures and test parameters, such as discharge waveforms. Simulator waveform verification can be integrated into a test flow, and drifts can be flagged from long term trend monitoring. It is possible to integrate a current measurement into the testing, such that the ESD current of each pulse is recorded, and the current waveforms which caused an ESD failure are included in the test documentation.

Test speed
Test speed advantage can get larger for a complicated test flow that requires many different actions, or when the number of test points is high, or the number of same test samples is large.

8.8.2 Disadvantages of Robotic Testing

The main disadvantage of a robotic test is the difficulty of automatically monitoring various failures and the programming of the test points. Manual tests may be required to understand the types of failures for proper automatic failure detection by a robotic tester, or the robot is used for repeatable testing, while an operator observed the DUT for failures. In addition, few companies offer robotic test systems and the cost of such systems may be prohibitive for many companies.

Appendix A: Body-worn Equipment

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Yingjie Gan, MS&T EMC laboratory

The core difference between the postures assumed for IEC 61000-4-2 human metal discharge and a discharge to a wearable device is the impedance between the charged body and the grounded structure discharged to. This leads to much higher currents for the same voltages [Zho2018, Ish2015, Ish2016, Ish2017 and Koh2018]. The difference in impedance is a result of the geometry. This is especially true for the waist worn device in which a larger portion of the body is close to the grounded structure, thus the geometry forms a much lower impedance (higher capacitance) which will lead to higher currents, see Figure A1.

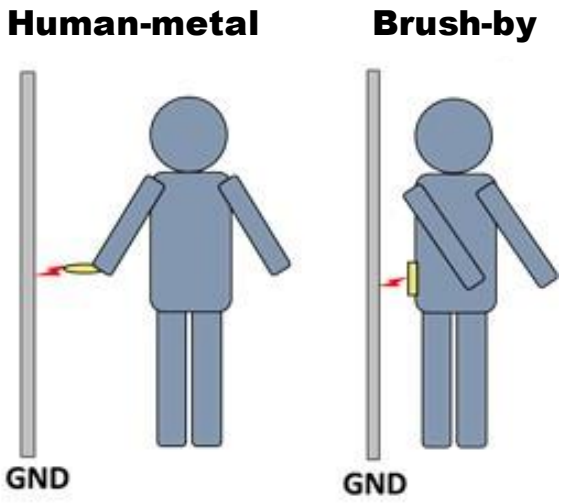

Figure A1: Different ESD scenarios for Brush-by and Human-metal Discharge

The discharge currents for different positions of the body-worn devices at 1 kilovolt are shown in Figure A2. The peak current for the body-worn devices are higher than the human-metal discharge case. The current for the waist-worn device can reach levels twice as high as in the human-metal discharge scenario as shown in Figure A3.

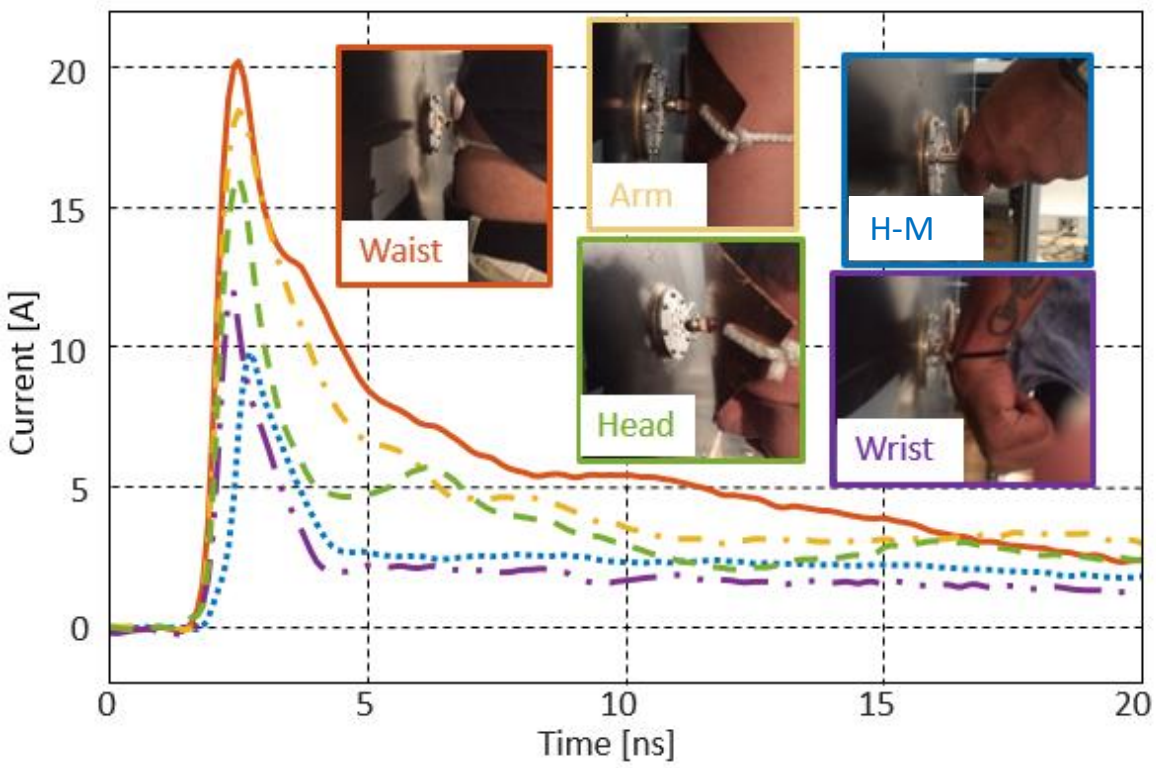

Figure A2: Discharge Current for Human-metal and body-worn Devices at 1 kV.

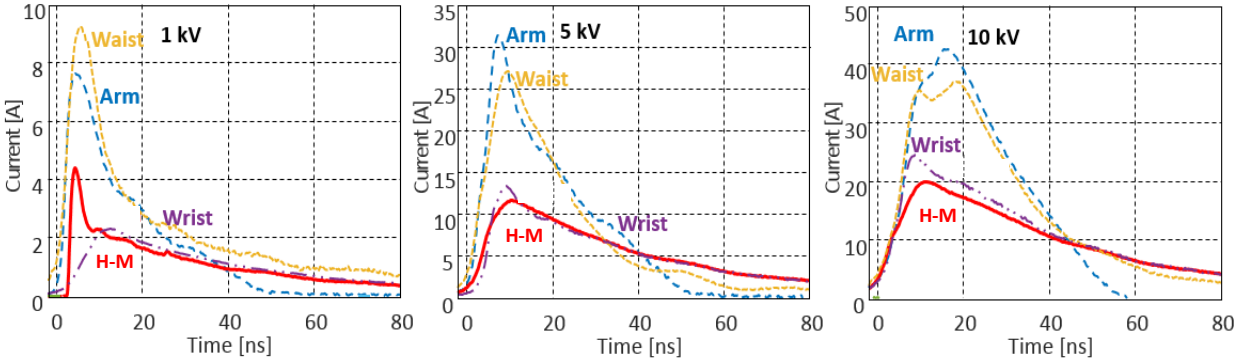

Figure A3: Discharge current for Human-metal and body-worn devices at different voltage levels.

When the voltage level increases, despite the variability for the air discharge, in most cases the current will be higher than 3.75 A/kV as specified for contact mode ESD. The current levels of the body-worn devices measured in the brush-by scenarios indicate the IEC 61000-4-2 standard setup is probably insufficient for ensuring the robustness of body-worn devices.

The capacitance variations need to be investigated for the cases when there are clothes or a plastic enclosure between the device and the human body. Data for a moist thin cloth or direct contact lead to similar waveforms. A dry insulating cloth and the data obtained using a 0.5 mm plastic insulator show similar waveforms at 1 kilovolt as shown in Figure A4. The insulation between the device and the body changes the total capacitance, but little effects were observed on the peak value or the rise time.

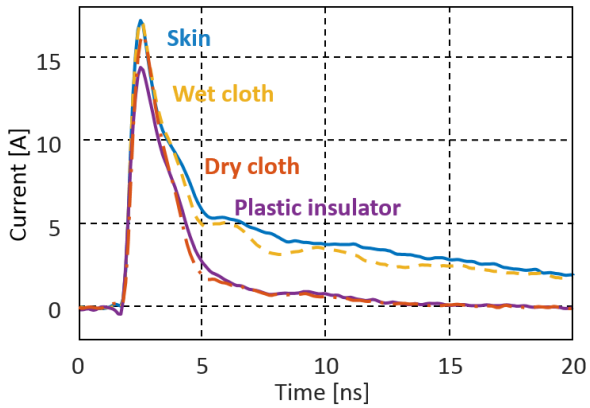

Figure A4: Discharge current for different connections at 1kV for waist worn device

The impedance formed by the body and the vertical ground plane can be used to determine the step response under the assumptions that the spark acts as an ideal switch and linearity. The impedance is measured using a vector network analyzer for different positions of the body-worn devices (see Figure A5) using a coax connection having the same dimensions as the ESD current target to ensure similar postures during the impedance measurements and the current measurements.

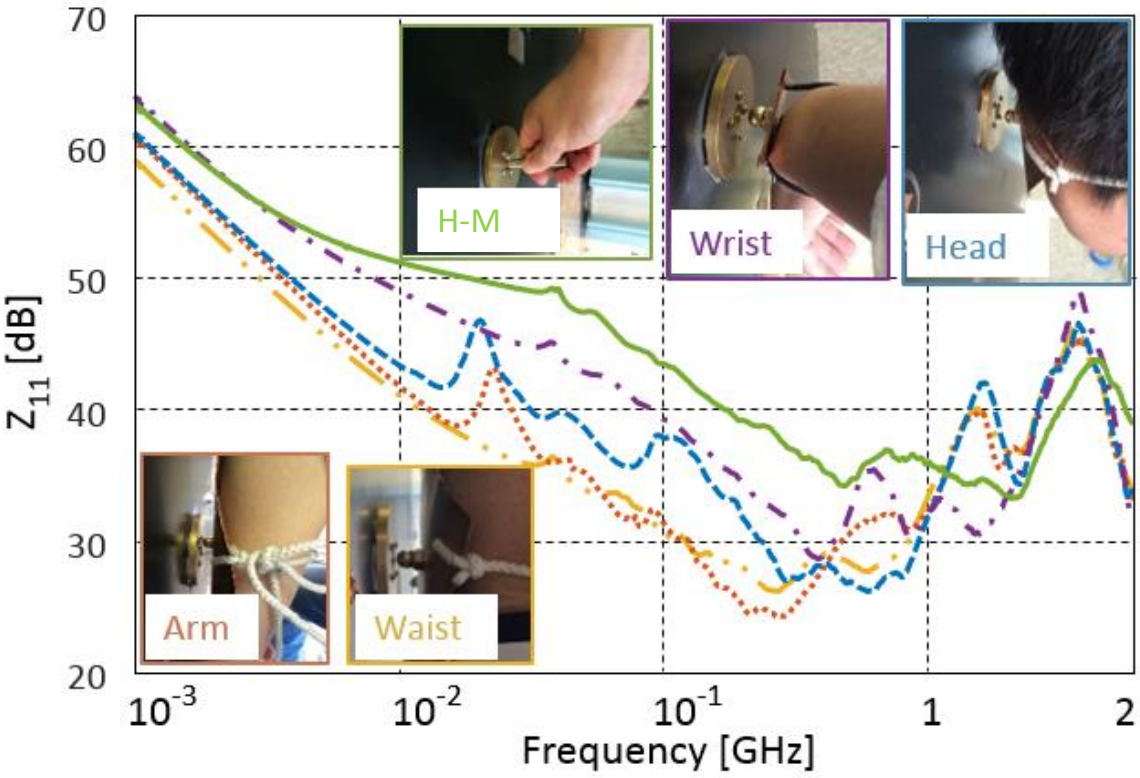

Figure A5: Measured Impedance Z_{11} for different positions of the wearable devices versus Frequency. Observe the capacitive behavior at lower frequencies, and the more complex behavior at higher frequencies caused by the local geometry around the discharge point.

By assuming that the spark is an ideal switch, the current can be reconstructed using the measured impedance. A 1 kilovolt step voltage source is used as excitation, the reconstructed currents for different positions are shown in Figure A6. The larger value of the current peak of the simulation data results from the assumption that the spark is an ideal switch. Simulations that model the actual time dependent spark resistance using Rompe and Weizel's spark resistance law can provide a better match to the measurements. For a system design, the main lesson is that the currents can be much larger than the currents during the IEC 61000-4-2 testing for the same voltage. The reason is the local impedance, which is much higher for a handheld metal part, relative to waist mounted metal.

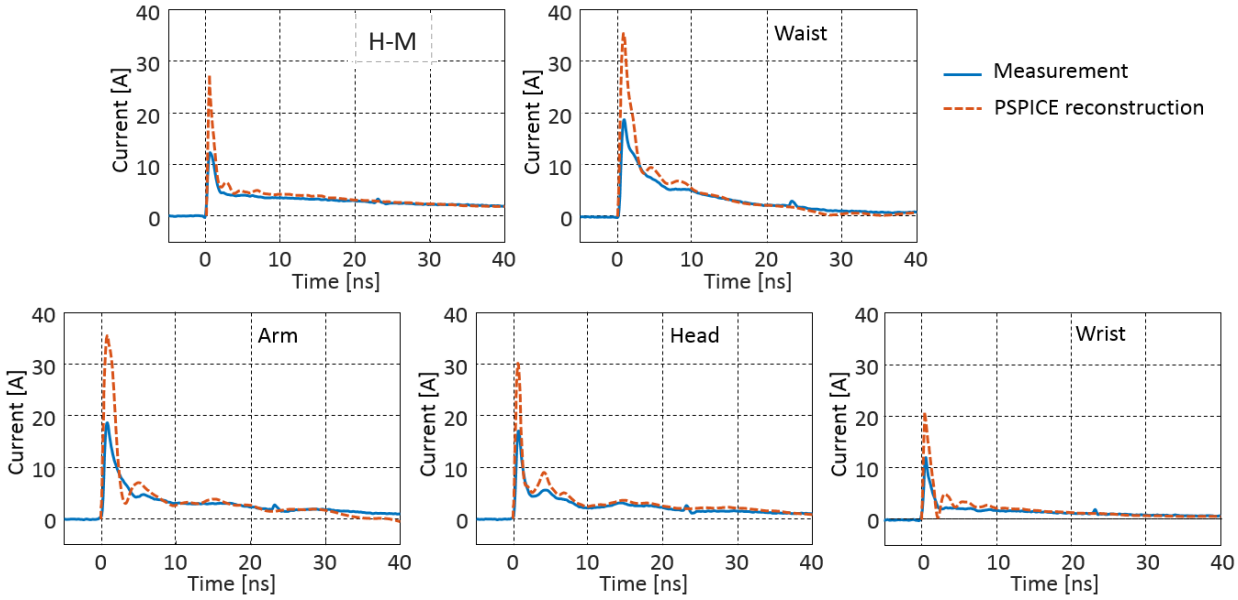

Figure A6: Comparison of currents obtained using PSPICE with measurements for different positions of the wearable devices and Human-metal discharge scenario at 1 kV.

The impedance can be approximated as an RLC circuit as shown in Figure A7. The parameters in the RLC models are tuned to achieve the best match with the measured impedance for each position, the values of the RLC parameters are shown in Table A1. C1 describes the capacitance of the body to ground. It dominates the impedance behavior in the frequency range from 1 MHz to 200 MHz.

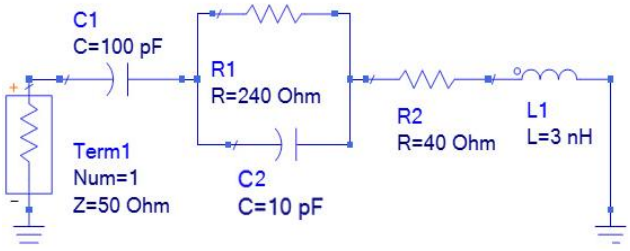

Figure A7: RLC model for Human-metal Discharge.

Table A1: RLC Parameters of the Wearable Devices Modeling for Different Positions

Position	R1 [Ω]	R2 [Ω]	C1 [pF]	C2 [pF]	L1 [nH]
Waist	240	24	220	150	4
Arm	380	20	220	125	9
Head	220	24	150	40	8
Wrist	350	29	120	20	8
H-M	240	40	100	10	3

After developing the linear parts of the models, the spark resistance is taken into consideration during the simulation. It has been shown that Rompe and Weizel's law can provide good predictions for the spark resistance having a spark length around or lower than the Paschen's value.

$$r(t) = \frac{l}{\sqrt{2K_R \int_0^t i\left(t'\right)^2 dt'}}$$

where $r(t)$ is the spark resistance at time t, l is the spark length, and K_R is a constant that is related to the gas pressure and type. Typically, Kr = (0.5~1)× $10^{-4} m^2/(\mathrm{V}^2\mathrm{s})$.

An example is given for the waist-worn position at 10 kilovolts when the constant value is set to $0.5 \times 10^{-4}\, m^2/(\mathrm{V}^2\mathrm{s})$ for the Paschen case, see Figure A8.

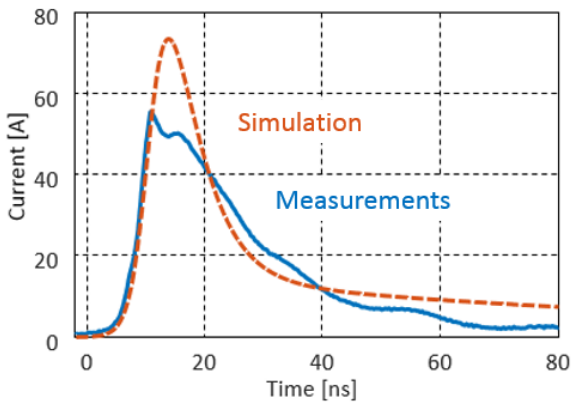

Figure A8: Simulated and measured current for waist-worn device at 10 kV, l = 2.7 mm, Kr = 0.5e-4 $\boldsymbol{m^2/(\mathrm{V}^2\mathrm{s})}$.

The current levels for the body-worn devices can be twice as high compared to the discharges from a handheld metal or the contact mode IEC 61000-4-2 specifications. This indicates that testing of body-worn systems according to the IEC 61000-4-2 standard may underestimate the real risk. Two possible solutions may ensure product quality. The first solution would be to use a higher voltage level in testing body-worn equipment. This will correct for the current magnitude, but it may cause a breakdown through plastic gaps that would not happen at the actual voltage. The second solution is to develop an ESD generator that better reflects the currents seen in body-worn equipment.

Appendix B: Display Testing

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B.0 Introduction

An electrostatic discharge can cause soft and hard failures of displays and touch screens [Koo2012, Kim2011, Li2106]. It is not possible for the spark to penetrate the glass, however, a variety of entry and coupling paths exists between the ESD and the display or its driving circuits [Shi2016].

The spark may reach the metal frame which is part of a flex cable connected display. If the edge encapsulation of the glass layers suffers an electrical breakdown, the spark may enter between the glass layers at the edge of the display into the touchscreen or display. If the display is not surrounded by a well-insulated structure, the spark may reach the flex cable, which connects the display to the main board. The spark may also reach other metallic structures around the display, such as the metal frame not connected to the display.

Especially in cases in which the spark can reach the flex cable or the encapsulation between glass layers, it will damage or upset the display. However, many designs surround the display with insulating structures, such that no direct discharge to a grounded structure is possible. For such a well-designed display, no sparking would be observed if a discharge to the display is attempted using an ESD generator in air discharge mode. However, not observing a spark often leads to the false conclusion of not having a current flow. The approaching ESD generator tip can cause surface charging that can reach currents of up to 10 amperes with <1 ns rise time.

During the IEC 61000-4-2 test the DUT is placed on a 0.5 mm insulating sheet, which is on the horizontal coupling plane (HCP). For discharge points on the back side of a phone this leads to a situation in which the display is facing the HCP. The capacitances formed between the phone and the HCP varies a lot depending on the on the size of the phone, its screen flatness, and the flatness of the insulator which may deteriorate over time. The regions with high local capacitance will receive more current, leading to reproducibility problems. Additionally, the possible corona at the edge of the phone can contribute several amperes to the current at higher voltage.

The discharges to the phone lead to a large displacement current flowing through the display. This current has multiple paths to the body of the phone: via the touch electronics, via the display electronics, and directly to the body of the phone. As these currents can reach 30 amperes (at 8 kV contact mode) they can lead to upset and damage of both the display and the touch layers.

The flatness of the insulating spacer is important. Currently, many laboratories use plastic that tends to wrinkle. This changes the distance to the DUT. If a polycarbonate plastic is selected, then a flat surface is created. It is suggested that for all tests in which the 0.5 mm thick insulator is used, a flat polycarbonate surface should be required.

B.1 Spark-less Surface Discharges

The corona current which spreads across the surface of the glass will cause a rapid change of the surface potential on the glass surface. This rapid surface potential change will cause a displacement current to flow via the capacitances to the inner structures of the display, such as, the touch layer or the display layer. These spark-less current paths are illustrated in Figure B1.

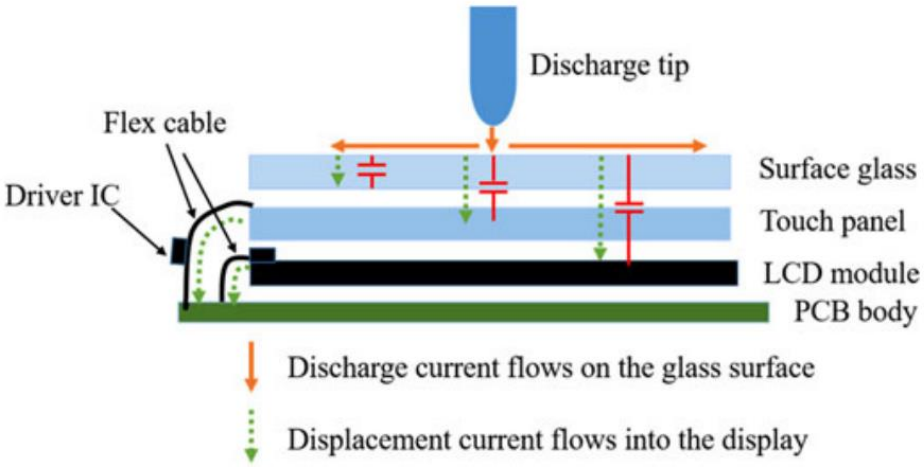


Figure B1: Spark-less surface corona current and displacement current paths into the display. The F-65 current probe is placed around the discharge pin.

The discharge current measured by the F-65 current probe at different voltage levels and polarities are shown in Figure B2. Because the displays' surfaces usually are made from insulating material such as glass or plastic, and discharges occur while a charged human is moving toward the display, air discharge mode was applied for this investigation.

The peak currents and total charges increase with discharge voltage level. The positive discharge current (about 11 amperes at +12 kilovolts) could be four times larger than the negative one (about –2.8 amperes at –12 kilovolts) while the rise time is similar (about 1 ns).

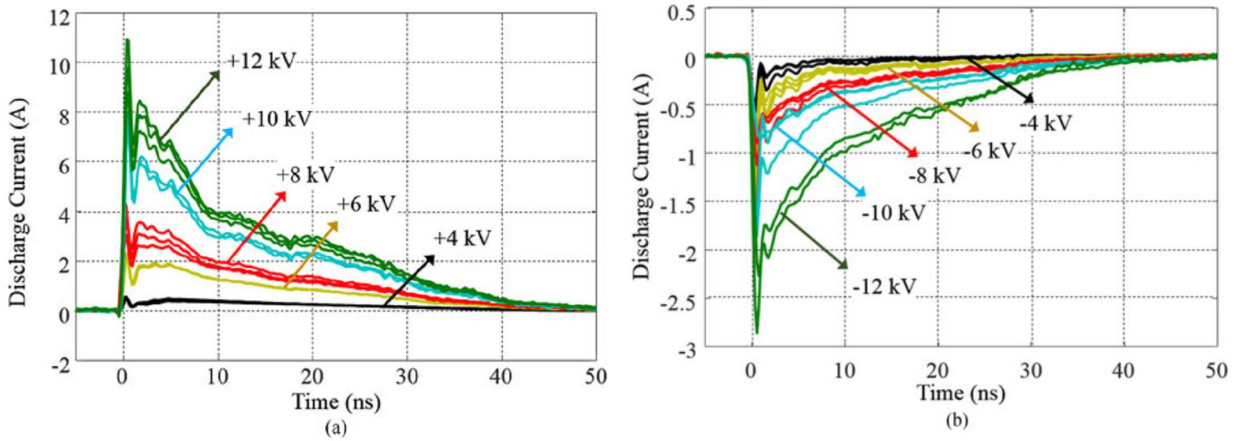
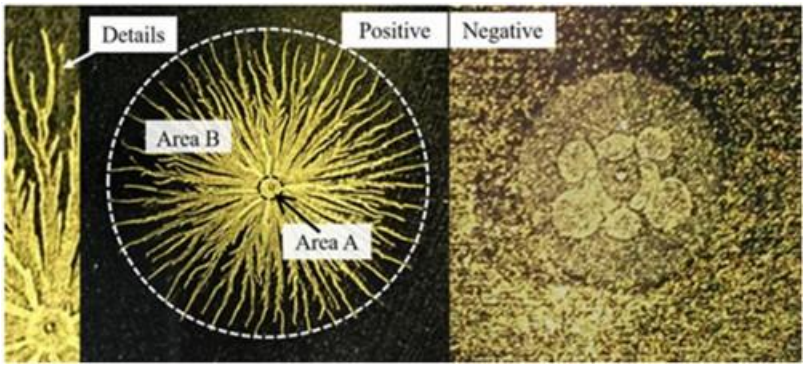


Figure B2: Discharge currents for different voltage levels and polarities, ESD generator discharge in air mode, 0.3 m/s approach speed: (a) positive and (b) negative discharge. Each voltage level was tested two to three times for repeatability resulting in multiple waveforms for each voltage level.

Lichtenberg's dust figure method can be used to help visualize the charge distribution and residual charges after surface discharging. An example is shown in Figure B3 for positive and negative discharges on a display. Area A is the corona discharge close to the electrode. In area B the streamers generate many branches, which are electron avalanche channels. Figure B3 (a) details a single branch. Typical negative dust figures do not show branching, see Figure B3 (b). The sizes of the negative dust figures are much smaller. This is due to the lower speed of the ions compared to the fast electrons dominating the positive discharge.



(a) (b)

Figure B3: Typical dust figures for (a) positive (note white circle is a 35 mm diameter) and (b) negative (note round area in photo is 15 mm diameter) discharges on a display.

In summary, spark-less surface discharges on displays can inject up to 10 amperes of discharge current at hundreds of picoseconds rise times which may upset or damage the display. These discharge currents depend strongly on the polarity, voltage level, approaching speed, humidity, and the surface glass characteristics. The detailed discussion can be found in "Experimental Characterization and Modeling of Surface Discharging for an Electrostatic Discharge (ESD) to a Liquid Crystal Display (LCD)"[Gan2017].

B.2 IEC Test for Display Face Down

The general set-up situation is shown in Figure B4. The phone is placed on the HCP. The discharge to the body of the phone will force displacement current from the body of the phone to the HCP and via the resistive / inductive networks of the display and the touch layers to the HCP.

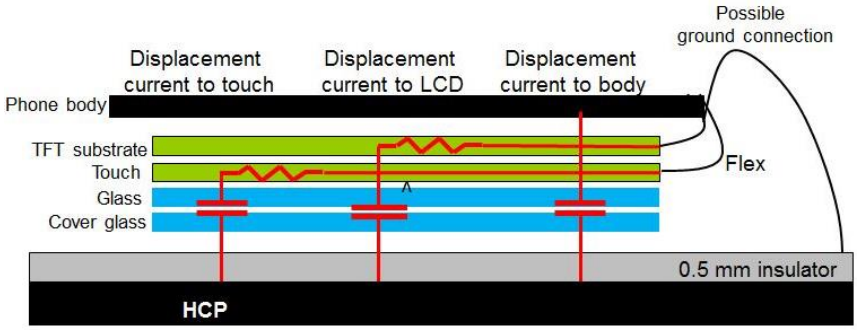


Figure B4: General setup of a phone or tablet in the display down configuration and indication of possible current paths. The F-65 current probe is placed around the discharge pin.

The currents depend strongly on the flatness of the insulating layer. The experimental results comparing the discharge currents when the cell phone is under different configurations, as shown in Figure B5, reveals the capacitance variations. The currents are measured using an F-65 current probe.

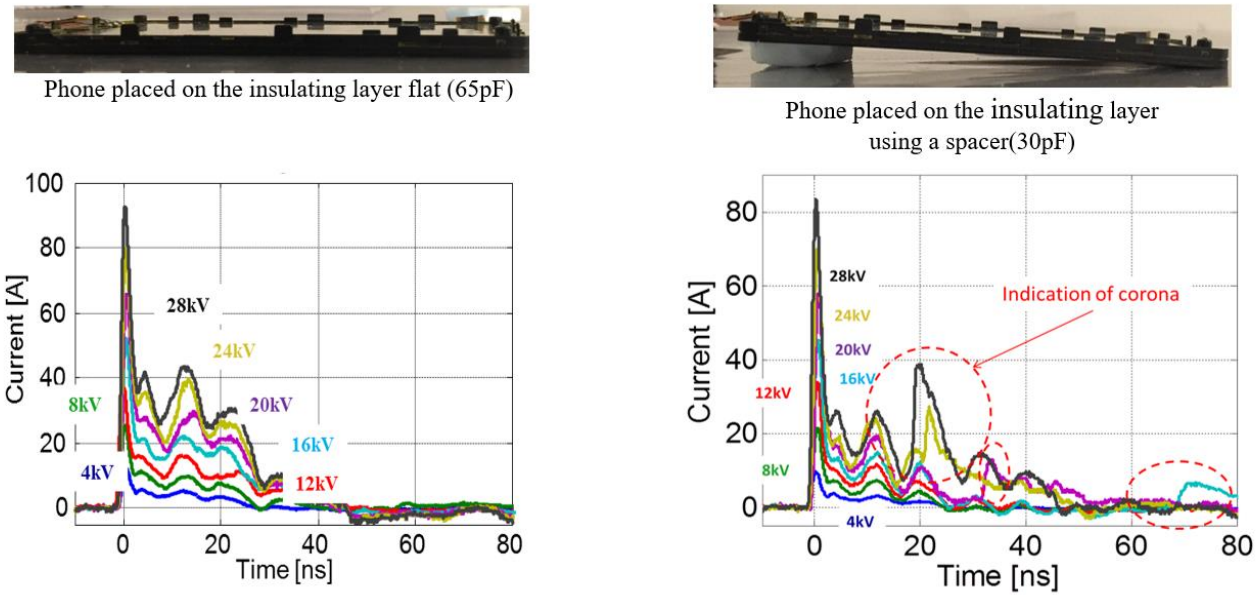


Figure B5: Currents for different arrangements of the phone.

A nonlinear current rise around 20 ns after the peak, indicating corona discharge, is shown in Figure B5. Corona is a process that does not repeat well, this will also lead to the low repeatability of test results if the response of the display is affected by the corona. Thus, test setups which are prone to corona should be avoided. In general, corona caused by surface discharges on the thin plastic layer covering the HCP need to be considered for higher voltage ESD.

For higher test voltages, the voltage between the HCP and the phone is large enough to cause corona discharge on the insulating layer, shown in Figure B6. Surface discharges will cause additional currents at the edge of the phone and can spread multiple centimeters away from the phone. Prior to starting, the 0.5 mm insulator needs to be free of any surface charge.

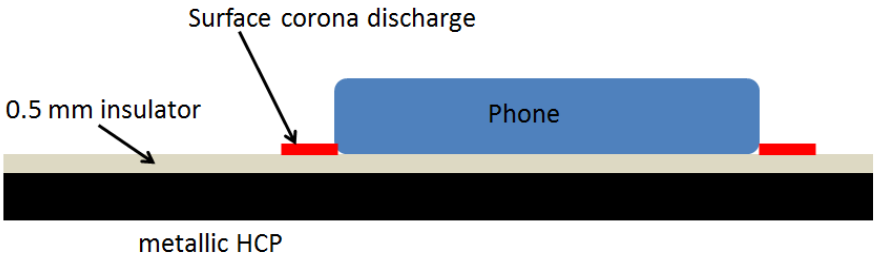


Figure B6: Illustration of the surface discharges along the top surface of the insulating layer used on top of the HCP.

The charges deposited on the surface can be visualized by using the Lichtenberg dust figure method. An example of such charge deposition measured at 25 kilovolts is shown in Figure B7 and Figure

B8. The phone is lifted from the HCP after discharge and the dust deposited. The surface discharge begins at around 20 ns after the initial pulse and, according to the measured data, adds tens of amperes which can increase the likelihood of fused bridges in the touch screen layer and other damage or upsets in the touch and the display.

The corona discharges form tree-like structures. Their propagation velocity is about 1 mm/ns and they can contribute to several amperes of additional current. A detailed photo is shown in Figure B8.

Figure B7: Distribution of charges on the insulating layer after discharging to a phone (display down). Charges deposited by corona discharge are visible outside the area the phone was placed in (white box).

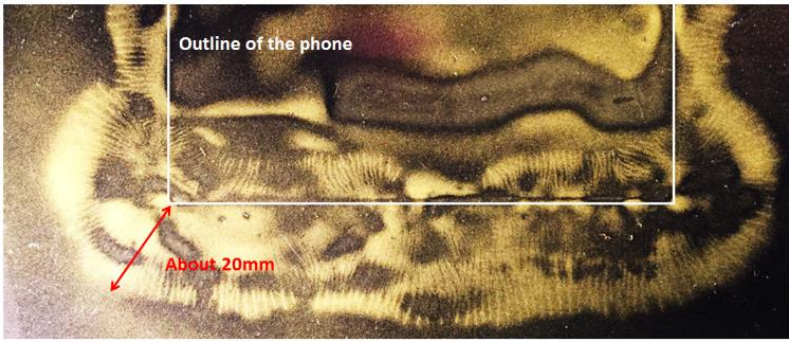


Figure B8: Detailed photo of the distribution of charges on the insulating layer after discharging to a phone (display down).

As discussed previously, the upside-down test situation is somewhat unrealistic, as few phones or tablets will be placed on a flat metal surface in a display down position. Besides being unrealistic, the test set-up may also lead to difficulty in reproducing results as the capacitance depends strongly on the thickness and flatness of the insulator used on the HCP. Increasing the insulator thickness to 5 mm is suggested for display down testing as it is more realistic to real usage. There would be less capacitance variations due to the flatness of the insulator. The corona will be less likely to occur due to lower field strengths. Fewer failures of the display would be expected, allowing introduction of advanced display and touch technologies faster. This only reduces the failure rate for the present

un-realistic face down test. The ESD risk caused by discharges to the display (spark-less) is still included in the test sequence of the IEC 61000-4-2 standard as air discharge to the display must be performed.

Appendix C: Investigations into Triboelectric Charging of Cables

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C.1 Investigation on Triboelectric Charging of Cables

In this appendix, the details regarding the measurement sequence and the relationship of cable charging to CDE events is discussed.

C.1.1 Test Preparation and Discussion

Inside a climate chamber, a Faraday cup was used to measure the charge that cables accumulated after they had been rubbed against a sweater for about 5 seconds. The test sequence included:

1. Store all materials inside the chamber for at least 24 hours to allow the humidity to equalize within the materials.
2. Rub the cables against a sweater for a few seconds.
3. Measure the accumulated charge using the Faraday cup.
4. Repeat the measurement five times to check repeatability.
5. Adjust the environmental conditions in the chamber to test repeatability and dependency on humidity.
6. Identify the highest charge and voltage levels.

As shown in Table C1, four different sweaters were used, each having a different level of charge affinity (as based on the triboelectric series). Even though the main cable of interest in this work was USB 2.0 (29 cables tested), other cables were also tested (3 USB mouse cables, 3 digital visual interface (DVI) cables, 2 coax cables, 2 coax RG400 cables, 6 banana cables, and 2 power cables). In total, 47 cables were tested.

Table C1: Sweater and materials according to the labels (taken from https://www.alphalabinc.com/triboelectric-series)

Sweater	Ingredient	Charge affinity (nC/J)
Orange sweater	100% Polyester	-10
Brown sweater	Wool and Nylon mix (50/50)	+30
Black sweater A& D	Wool and Acrylic mix (50/50)	-10
Black sweater	100% Cotton	+5

As is shown in Figure C1, the measurement setup consists of a charge cup loaded by a 10 nF capacitor. The charge accumulated on the cable, and the corresponding voltage, are obtained from Eq. (1) and (2), respectively.

$$\mathbf{Q}_{\text{cable}} = \mathbf{C}_{\text{Faraday-Cup}} * \mathbf{V}_{\text{DVM}} \quad (1)$$

$$\mathbf{V}_{\text{cable-Plug-in-Scenario}} = \mathbf{Q}_{cable} / \mathbf{C}_{cable} \quad (2)$$

Where $C_{Faraday\text{-}Cup}$= 10 nF and C_{cable}=20 pF. C_{cable} is the capacitance of a cable to ground or the capacitance between a person holding a cable and the cable's inner structure itself.

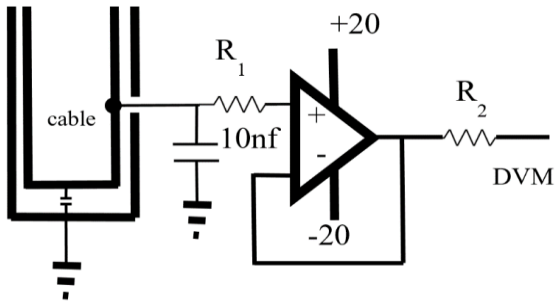

Figure C1: Measurement set-up, charge cup, and high impedance amplifier

To understand the uncertainty of the results, each test was repeated five times. Five different humidity conditions were studied as well. Although all tribocharging experiments on materials of normal daily use show large variations, it is of interest to identify general relationships between the charge and environmental conditions. The experimental results, effect of materials on charge, empirical relationship between charge and wet-bulb temperature, functional relationship between charge, relative humidity and temperature are explained in detail in [Rez2017].

C.2 Relationship to Cable Discharge Event (CDE)

To convert the charge levels into a voltage, a capacitance value must be assumed for the capacitance of the charged cable to ground. Based on measurements, 20 pF was selected. For any other capacitance value, the voltages would scale inversely to the capacitance. Using 20 pF, voltages were obtained for the plug-in cable discharge event. Figure C2 shows maximum and minimum voltages generated, versus wet bulb (WB) temperature, in USB cables for all sweaters. Figure C3 shows maximal and minimal generated voltages in all cables and four different sweaters. The largest voltage among all cables was -7 kilovolts, wet bulb (WB) = 6 ºC, by the combination of coax_58 (RG400) cable and *the Brown sweater*. The largest generated voltage for USB 2.0 was 4 kilovolts under WB = 6 ºC, using *the Orange sweater*. A secondary thought is needed to estimate the risk of upset or damage to an electronic system caused by inserting a cable charged to these voltage levels. As this study specifically focuses on USB 2.0 cables, one needs to take the connector specifications and the resulting pin sequencing into account. This is explained further in the USB cable plug-in measurements section of Chapter 2.

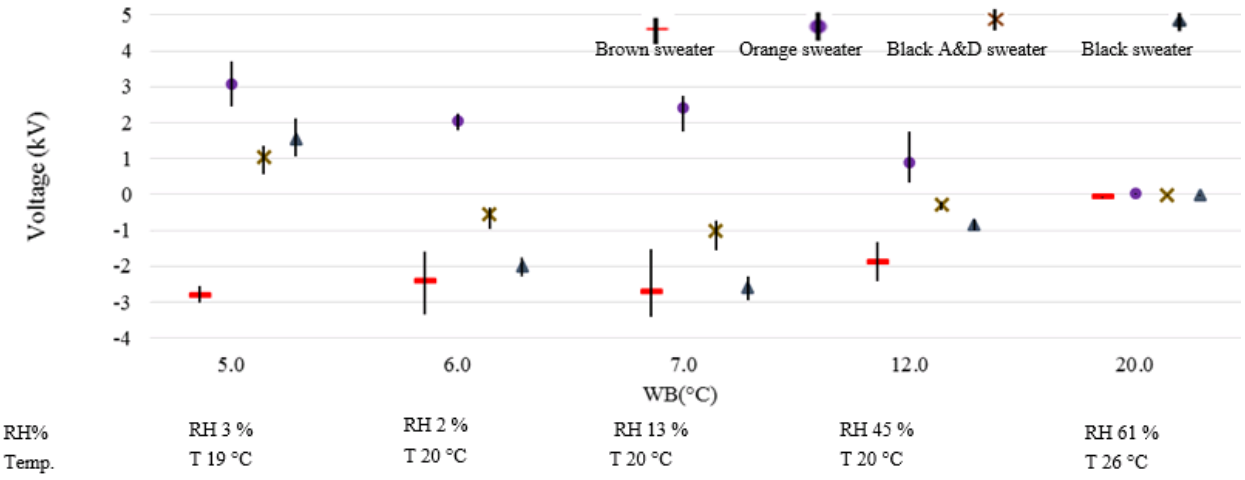

Figure C2: Maximum generated voltage with USB cables using 20 pF cable capacitance

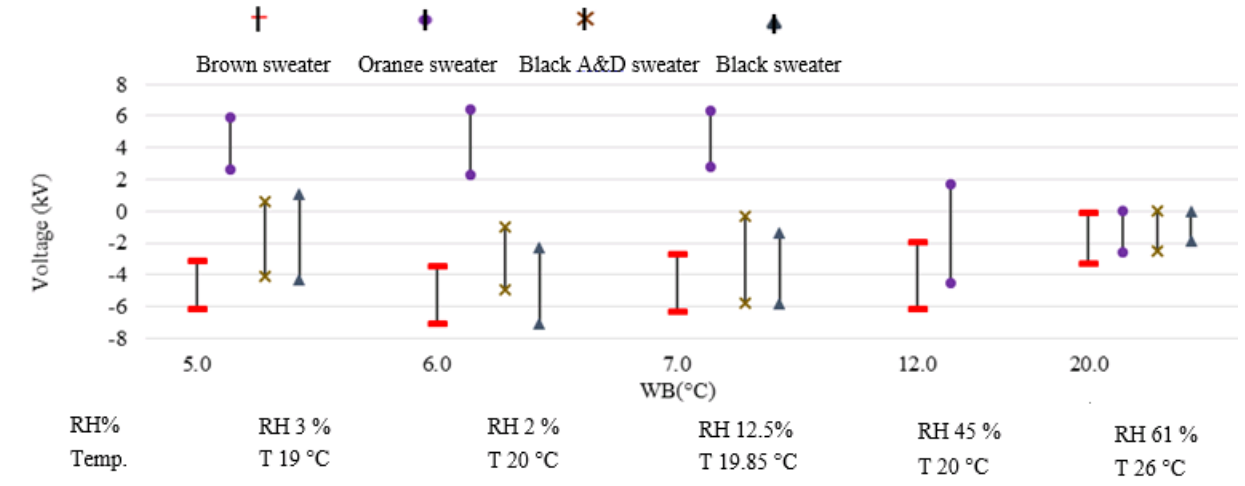

Figure C3: Maximum and minimum generated voltages with different sweaters versus WB temperature using 20 pF cable capacitance.

Appendix D: ESD Generator Full-wave Simulation Models

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D.1 Full-wave Based ESD Generator Models

Full-wave modeling of system level ESD is of interest for predicting ESD behavior in complex systems. A full-wave model solves an electromagnetic problem by implementing Maxwell's equations. Thus, it contains the coupling between the time changing magnetic field and the time changing electric field. In most cases the prediction is not absolute, but relative, asking if a design variant will improve the robustness, and if yes, by how much.

A complex system consists of multilayer PCBs for the electronic device and/or the system mechanical design of the device, including the connectors, LCD, battery, and chassis. In order to be able to simulate ESD phenomena in a complex system, a full-wave model of the ESD generator should be used. The full wave model may include the coupling of the transient fields, or it can be limited to just injecting the ESD discharge current. By using the full-wave model of an ESD generator, the field coupling to the system can also be predicted. If the simulation of ESD is done to predict a soft failure in the system, then the field coupling from the ESD generator should be considered in the simulation in most cases. Different full-wave ESD generator models have been presented [Cen2003, Wan2003 and Can2006a]. In the model presented in [Cen2003] which can be used with standard electromagnetic software [CST Microwave Studio], the structure was excited with a step function with a 1 ns rise time. In difference to a real ESD generator that does not model the relay and its associated low pass filters. Thus, radiation of strong ESD transient fields, with frequency components higher than 300 MHz caused by the fast voltage collapse (with 50~100 ps rise time) in the relay, was not considered in this model. A highly detailed model which was based on a finite-difference time-domain (FDTD) method has been presented in [Wan2003]. In this model (Figure D1), the currents and fields from an ESD simulator in contact mode were obtained by using the geometry and charge voltage. In the FDTD algorithm, the time-dependent material properties were controlled to model the physical stages of charging and discharging. This model shows the best accuracy, however, it required time dependent materials which are not a standard feature of most EM software.

A more detailed full-wave ESD generator model considering the details of the relay and the low pass filter has been presented in [Cai2008] (Figure D2). Although this model was verified by comparing some simulation results with measurements, the injected current into a large ground plane was not the same as measurement (Figure D3). In [She2014], a full-wave model of the ESD generator was developed and it was combined with the IC behavioral model to predict the failure of an 18 MHz D flip-flop IC.

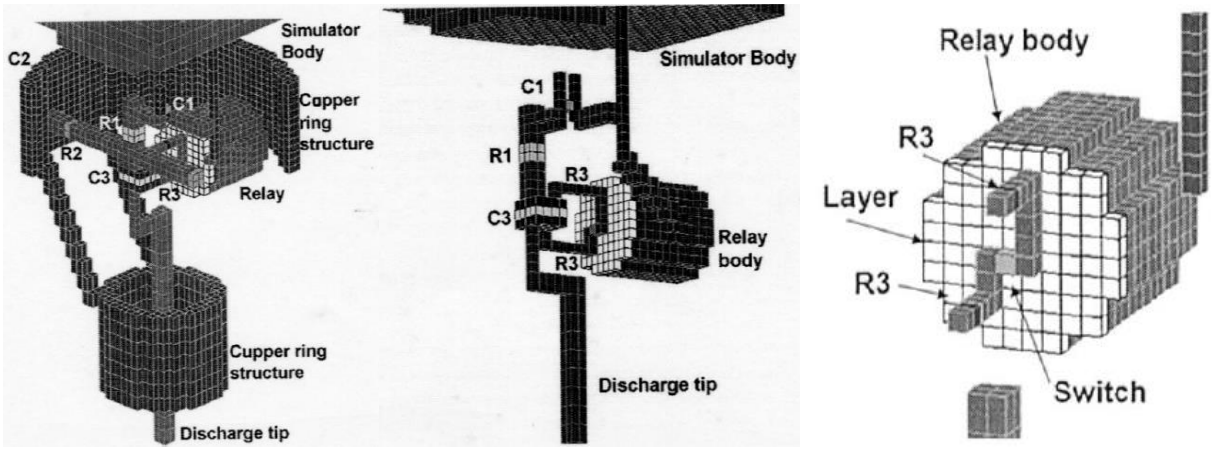


Figure D1: ESD generator model in [Wan2003].

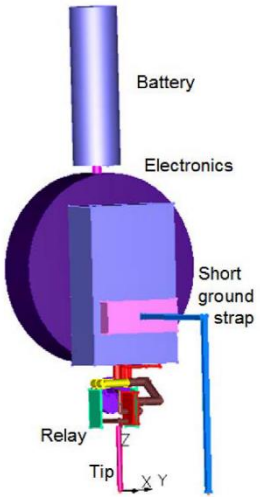
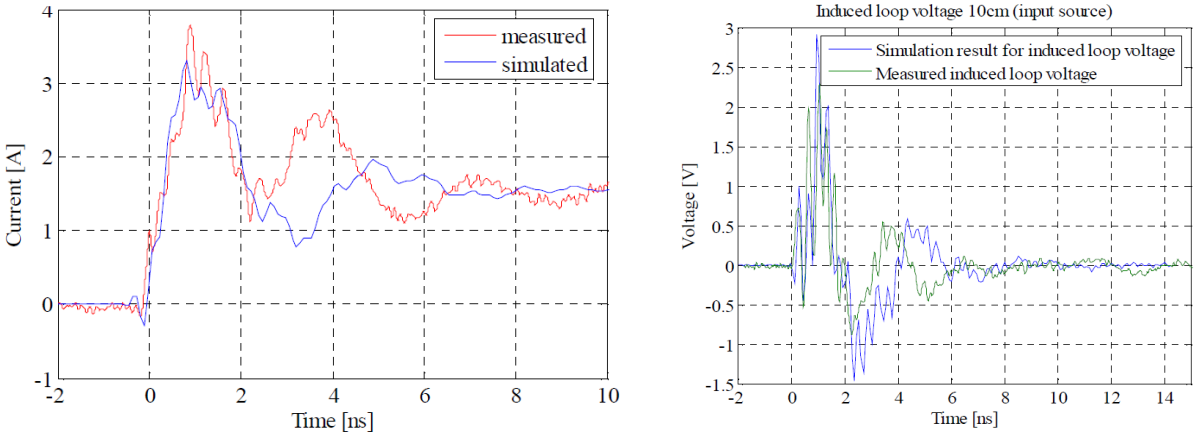


Figure D2: ESD generator full wave model overview [Cai2008].



(a) (b)

Figure D3: Simulated and measured (a) ESD discharge current, (b) induced loop voltage [Cai2008].

Although ESD generators from different manufacturers have almost the same injected current, they may excite significantly different electric and magnetic fields [Fre1998]. Therefore, for a full-wave model of an ESD generator to be able to simulate the transient ESD electromagnetic fields, the

model should be created based on the real ESD generator of interest. In [Liu2009], a full-wave model for the Noiseken ESD generator has been presented (Figure D4). This model was developed in Computer Simulation Technology (CST) Microwave Studio and could simulate the discharge current and transient fields of the ESD generator (Figure D5). The generator's individual components such as the relay, capacitor unit, coil, ferrite rings and polyethylene disks were accurately modeled in this work. This model was verified by comparing the simulated and measured discharge current and induced loop voltage. A full-wave model of the Teseq ESD generator has been created in CST Microwave Studio by MS&T EMC Laboratory in 2011 (Figures D6-D7). This model can simulate the transient electromagnetic fields precisely since the main components of the generator such as the relay, RC block and coil are considered in the model.

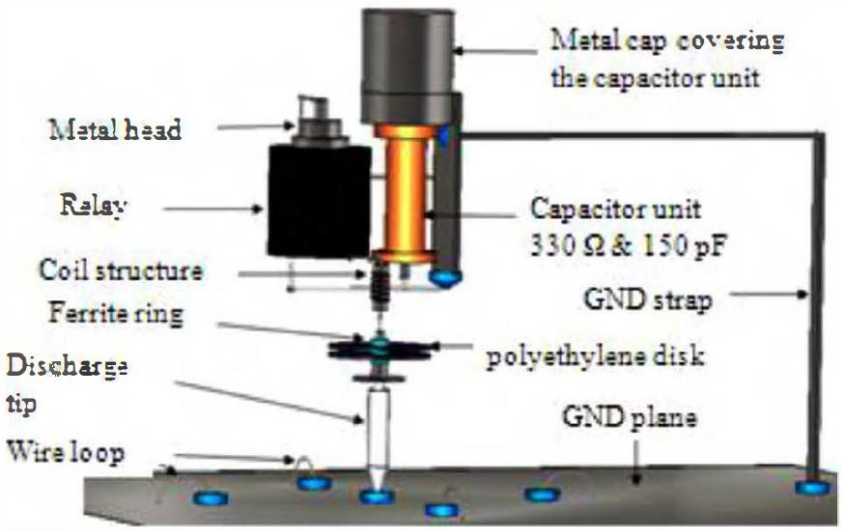
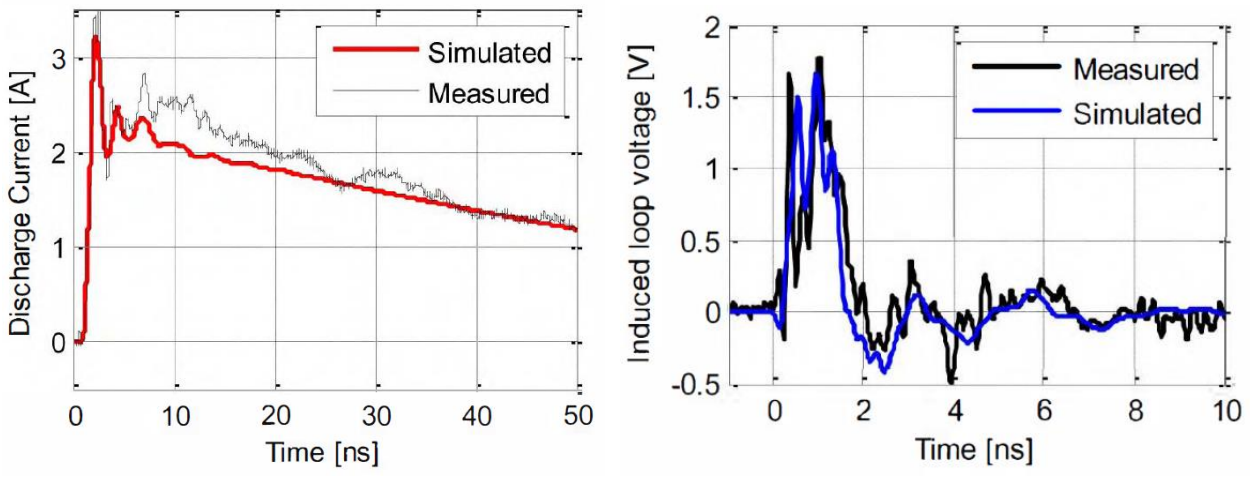


Figure D4: Full-wave model of Noiseken ESD generator [Liu2009].



(a) (b)

Figure D5: Comparison of the simulated and measured (a) discharge current, (b) induced loop voltage at 0 degree with 10 cm distance [Liu2009].

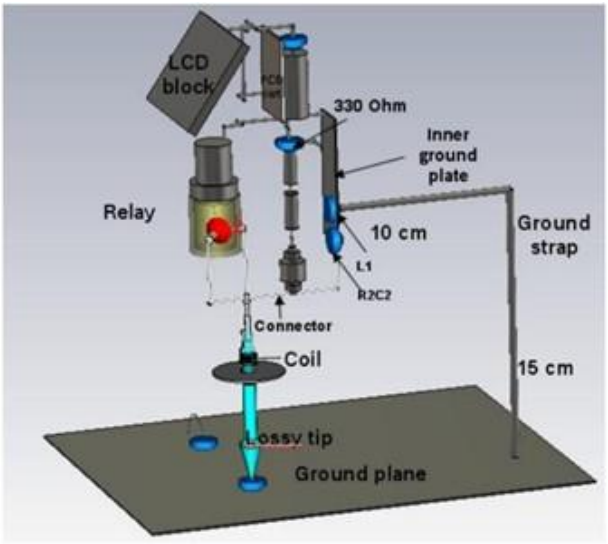
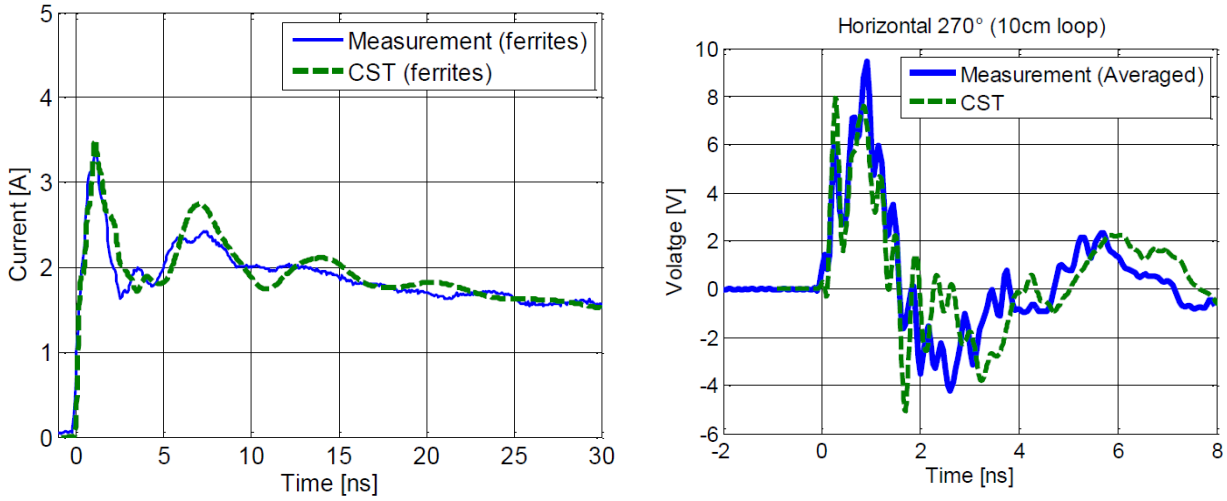


Figure D6: Full-wave model of Teseq ESD generator.



(a) (b)

Figure D7: Comparison of the simulated and measured (a) discharge current, (b) induced loop voltage at 10 cm distance for Teseq ESD generator.

If the ESD injection into a complex system is investigated, the transient fields of an ESD generator are often not necessary. It is enough to consider only the ESD injected current in the full-wave model. For this case, another ESD generator model was developed by MS&T EMC Laboratory which has reduced dimension (63x) and volume (90000 x) compared to the Teseq ESD generator model. Figure D8 (a) shows the small ESD generator model. Due to its very small size, the less complex ESD generator model is suitable for modeling ESD injection into complex systems consisting of PCBs where there are many thin traces, vias, dielectric layers and passive components with affordable runtime. A comparison between the ESD current injected by the Teseq and the small ESD generators to a metal plate is presented in Figure D8 (b). A good agreement between the injected currents from both small and big models is observed.

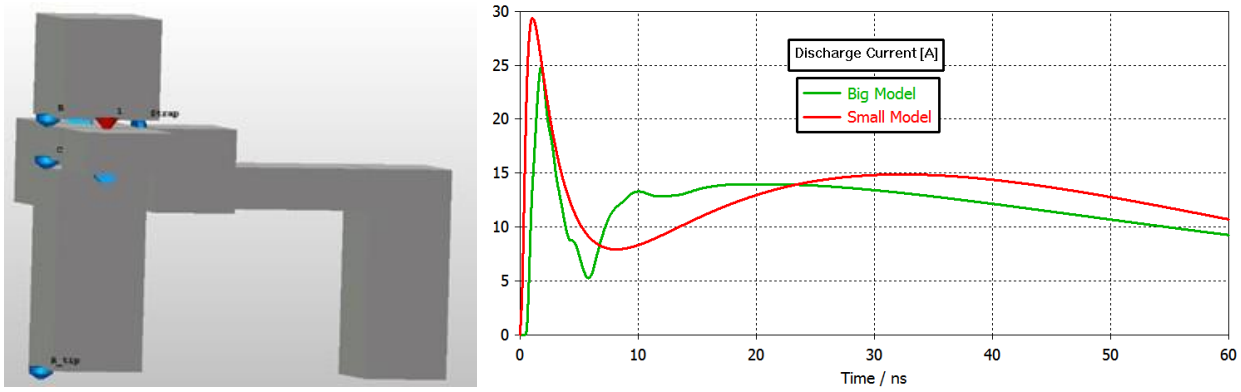
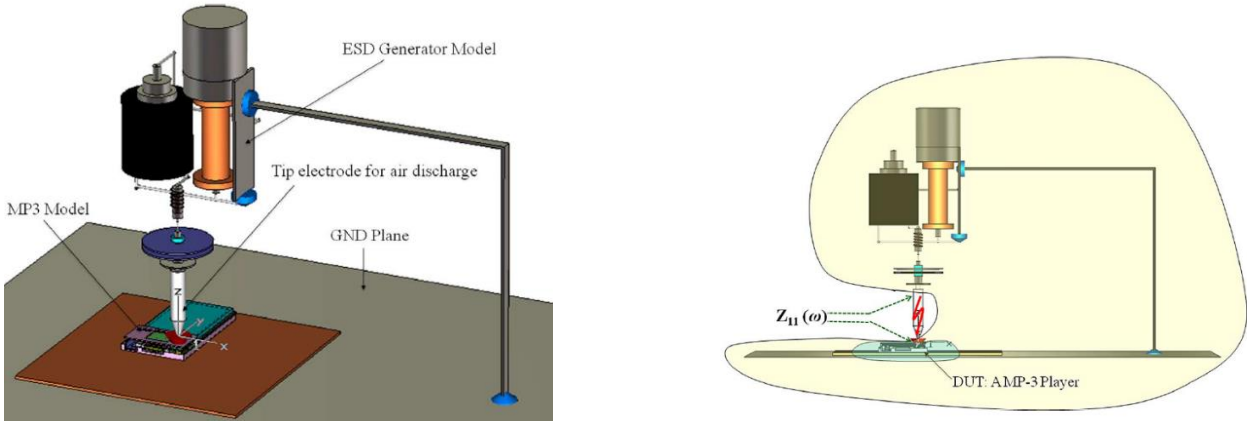


Figure D8: (a) Full-wave model of small ESD generator, (b) comparison of the injected current by Teseq and small ESD generator models.

Besides using the full-wave models of ESD generators in simulating ESD in contact discharge mode, these models can also be used in simulating air discharge ESD. In [Liu2011], the Noiseken ESD generator model presented in [Liu2009] has been used to simulate an air discharge ESD into an MP3 player (Figure D9). In this work, the linear ESD generator model was combined with the nonlinear arc resistance model and the currents and fields in air discharge mode were simulated (Figures D10 and D11). In the presented method, first the S-parameters of the linear section of the circuit were obtained from the full-wave simulation. Then, they were combined with the nonlinear part of the circuit in SPICE. In this method, the S-parameters were obtained once, and they could be reused when only the arc parameters were changed. In [Li2017], two methods of simulating the air discharge ESD current and fields have been presented by using the Teseq ESD generator model developed by the MS&T EMC Laboratory. The setup, which consisted of a discharging rod, is shown in Figure D12. The first simulation method was a two-step process in which the impedance between the tip of the rod and the ground was first simulated and then they were combined with the arc model in a circuit simulation. This method was the same as the work presented in [Liu2011] but the ESD generator model and the measurement setup are different. In the second method, the simulation was combined with the arc resistance of Rompe-Weizel (RW) directly by exchanging the voltage and current information in every time step. In this method, the transient electromagnetic co-co-simulation of CST Microwave Studio was used to simulate the currents in the discharging rod. The simulation simultaneously solved Maxwell's equation in the time-domain and the arc-resistance equation to estimate currents and fields for a given geometry, voltage and arc-length. It was shown that the simulated currents and current derivatives obtained from the presented methods matched well with the measurement results.



(a) (b)

Figure D9: (a) Full-wave model of the Noiseken ESD generator and MP3 player (air discharge mode), (b) location of Z11 port [Liu2011].

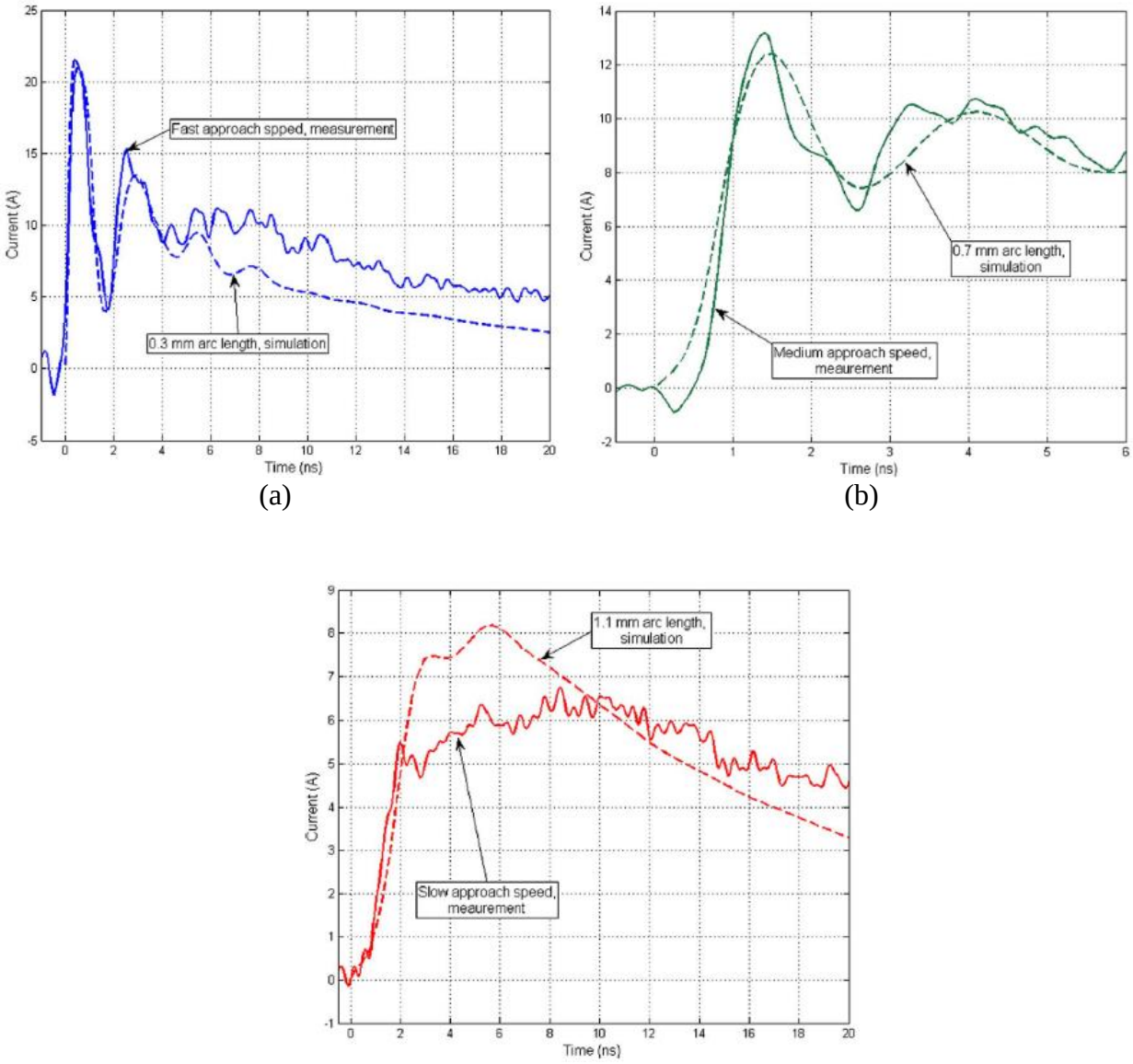


Figure D10: (a) Simulated discharge current for a 0.3-mm arc length and measured current for a fast approach speed, (b) Simulated discharge current for a 0.7-mm arc length and measured current for a medium approach speed, (c) Simulated discharge current for a 1.1-mm arc length and measured current for a slow approach speed [Liu2011].

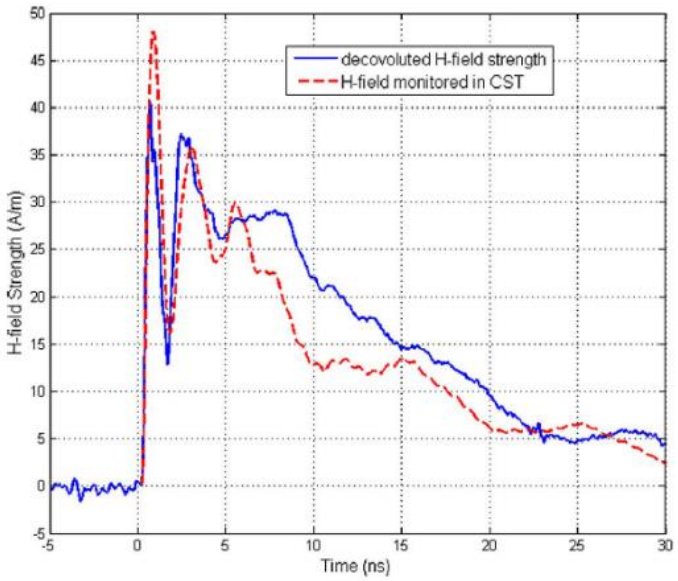


Figure D11: Measured and simulated magnetic field at 5 cm away from the discharge point [Liu2011].


Figure D12: Test setup of the air discharge experiment in [Li2017].

When a full-wave ESD generator model is used to simulate ESD into a complex system, the proper solver of the full wave electromagnetic simulator should be used. Both frequency- and time domain solvers may be suitable. Each offers a set of advantages.

If the geometry can be gridded into hexahedral grids (meaning that grid lines are parallel to the X,Y and Y coordinates, but the distance between grid lines can change throughout the volume) then time domain solvers might be superior relative to frequency domain solvers as the time domain solvers can solve rather large volumes without facing memory issues. Additional advantages can be offered by different methods to reduce the number of cells after initial gridding. Here each vendor has its own methodology, such as sub-gridding, partially filled cells, and the 'lumper' in the transmission line method that combines cells and often reduces the number of cells by 99% or more.

If the structure has curvature or, e.g., two PCBs are arranged at a 30° angle to each other, the hexahedral grids will need very many cells. In these cases, frequency domain solvers will be attractive. These offer automatic iterative meshing and often lead to more accurate results. Both methods allow the inclusion of linear and non-linear circuit components. This can be achieved by calculating the linear part of the geometry first to create a linear S-parameter description that is then used in a circuit level time domain simulation in conjunction with the non-linear components, or

the inclusion of non-linear components can be performed in lock-step during a time domain full wave simulation. This whitepaper cannot give a judgement as to which methods are superior, it can only encourage researching different methods and to identify the best method for the specific problem at hand.

CST Microwave Studio has two different time domain solvers: finite integration technique (FIT) and transmission line matrix (TLM). FIT is based on a consistent discretization scheme of an integral form of Maxwell's equations while TLM is based on the analogy between field propagation and transmission lines where the computational domain is considered as a mesh of transmission lines interconnected at nodes. The main difference between these two-time domain methods from the user point of view is the discretization of the structure. Unlike FIT, TLM utilizes a sub-gridding based on the geometry which avoids discretizing the regions which do not need fine grids. Therefore, for structures consisting of regions which are not needed to be meshed with fine grids, using the TLM solver can save computational space and time. For some structures, both FIT and TLM take almost the same time and space, but for some structures the only possible solver which can be used is TLM. As an example of the FIT and TLM usage, the Teseq ESD generator model of Figure D6 discharged on a ground plane is simulated. The simulation information is summarized in Table D1. The comparison between the ESD injected current obtained from TLM and FIT solvers are given in Figure D13.

Table D1: Simulation information for the Teseq ESD generator discharged on a ground plane solved by CST FIT and TLM solvers.

CST Solver	# of meshcells		# GPUs used	Simulation runtime
FIT	5.8×10^5		2	10 minutes
TLM	before lumping 104×10^6	After lumping 4×10^5	4	10 minutes

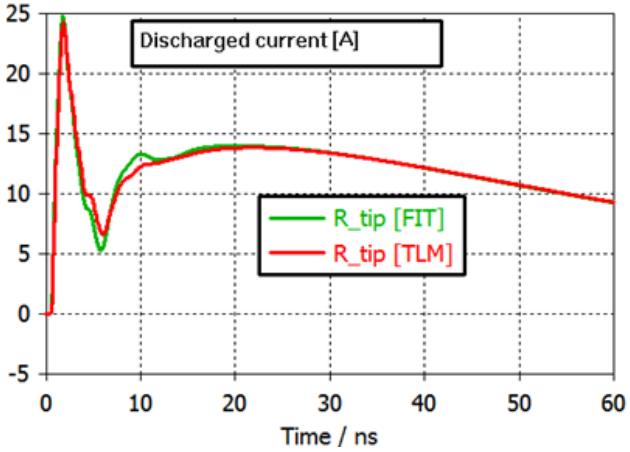


Figure D13: Comparison between discharged current on a ground plane obtained by CST (a) FIT and (b) TLM solvers.

Recently, MS&T EMC Laboratory worked on full-wave modeling of the secondary discharge in complex systems such as electronic devices [Mar2017a]. The developed model consists of the full-wave model of the Teseq ESD generator, a decorative metal in which ESD is discharged in contact mode, a metal screw mounted on the decorative metal and a current target at a distance from the tip of the screw. The distance between the current target and the screw is considered as the spark gap. One of the main challenges in developing this model was controlling the initiation of the arc resistance. In the circuit modeler of the FW simulator, a switch is used to control the on/off state of the Rompe-Weizel (RW) model. This is shown in Figure D14. This switch is necessary since the RW model does not have any explicit dependence on the Paschen value and requires decision making control to cause the initiation of the arc resistance. More details of the full-wave model can be found in [Mar2017a]. Table D2 summarizes the simulation results of secondary discharge parameters with the measurement results.

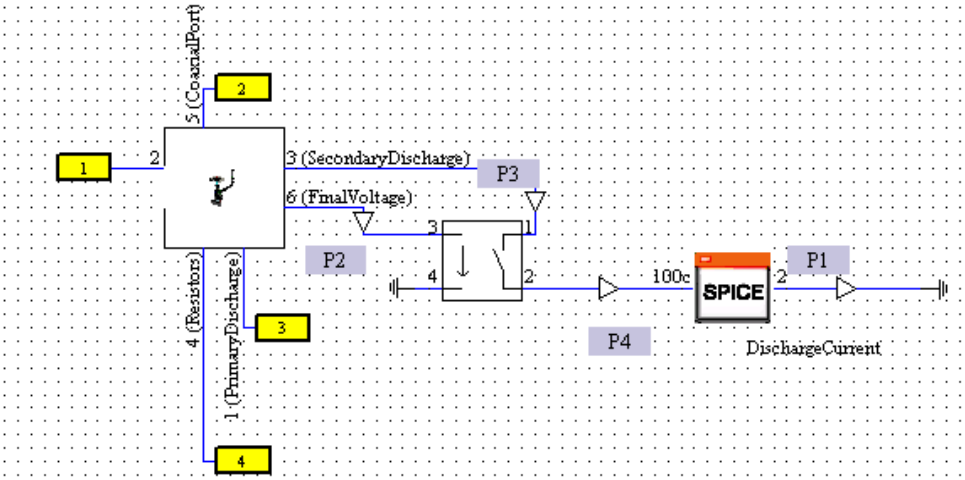


Figure D14: Switch-controlled RW model implementation in the circuit modeler of CST.

Table D2: Comparison of simulation and measurement results for the secondary discharge on the decorative metal [Mar2017a].

Parameters for 6 kV at 0.8 mm spark gap	**Measurement**	**Simulation**
Primary charging current peak	20.96 A	18.98 A
Primary charging current rise time (20% - 80%)	650 ps	550 ps
Secondary ESD peak current	68.73 A	82.18 A
Secondary ESD current rise time (20% - 80%)	550 ps	520 ps
Statistical time lag between the primary charging current and Secondary ESD	61.1 ns	5.05 ns
Paschen breakdown voltage	3.910 kV	3.910 kV
Peak metal plate voltage	5.58 kV	4.74 kV

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Revision History

Revision	Changes	Date of Release
1.0	Initial Release	September 2020
1.1	Address typos in Sections 3.3, 5.3.2, 6.1.11 & D.1, updated JEP equivalent document to JEP163, logo page updated	May 2021